BIT-MAP GRAPHIC DISPLAY CONTROLLER

GENERAL DESCRIPTION

The BPCRT2 is a CMOS Color Display controller intended for cost effective bit-map oriented applications. Display resolution and number of bits per pixel are software programmable.

The device can drive directly up to 2 Megabytes of memory and provides the necessary refresh for the DRAM devices. In order to minimize the number of integrated circuits necessary in a minimal application, several system control functions are also integrated. Used with the 68070 in a minimal configuration, it controls the access to the System/Video DRAM, to the System ROM and to the I/O devices.

A high speed pixel manipulation circuit can accelerate the image manipulation compared to performing this by the central processor alone. An interface for a graphic co-processor is implemented to allow very high speed manipulation of the video memory contents.

FEATURES

- Full Bit-Map organisation
- Capability to display Run-Length coded files
- Direct interface for 68000 compatible CPUs
- Up to 768 x 560 screen resolution
- 4 or 8 bits per picture element
- Mosaic effect
- Shift register for up to 15 MHz pixel rate
- On-chip oscillator
- Synchro generator for 50 and 60 Hz scan
- Double frequency scan
- Synchronisation with external video
- 1.5 Megabyte DRAM direct drive
- 0.5 Megabyte ROM control
- Reset sequencer, Watch-Dog timer
- Fast 16-bit pixel test-and-modify logic (pixblt)
- CMOS technology
- Surface Mounting Device package

APPLICATIONS

- Home Computer
- Personal Computers
- Home entertainment
- Intelligent color terminals
- Graphics/text I/O systems

PACKAGE

- 124-pin QUAD FLAT PACK plastic

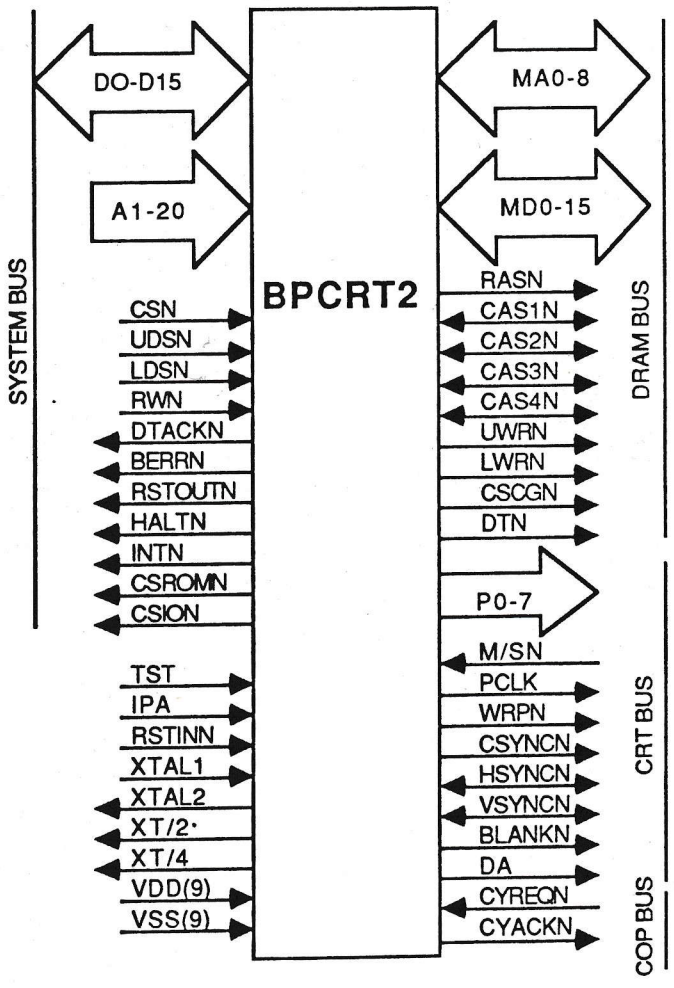


FIGURE 1: : LOGICAL PIN DESCRIPTION

BLOCK DIAGRAM

The following diagram describes the general organisation of the device.
The connection to the system bus is made via 16 bidirectional Data lines, 20 Address lines and CONTROL lines.
The connection to the Dynamic RAMs is made via 8 or 9 ADDRESS lines (MA bus), 16 Bidirectional DATA lines (MD bus) and control signals.
The video output is made of 8 Video DATA lines and 2 control lines.
The pixel accelerator is accessable both from the system bus, eg. using the CPU, and from the memory bus, eg. using the coprocessor interface.

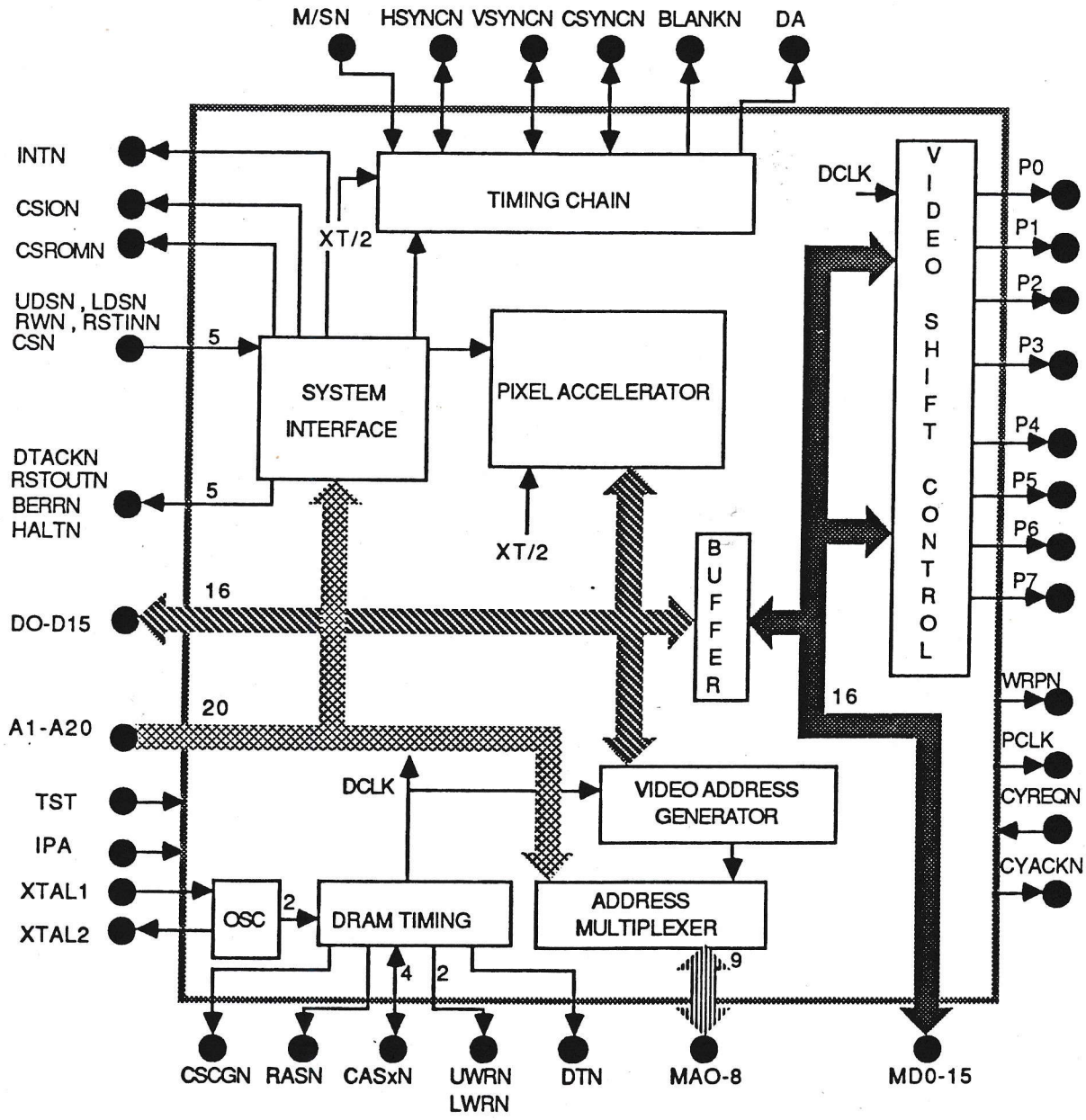


FIGURE 2: GENERAL BLOCK DIAGRAM

X pull-up RSTOUT, HALT, BERR, INT

PIN ASSIGNEMENT

Name	I/O	pin number	Description
SYSTEM BUS			
A1-A20	I	34-33 30-18 16 14-11	System ADDRESS lines. Provides the system address for access from the system bus. Must be stable when UDS or/and LDS go Low.
D0-D15	I/O	42-45 47 49-51 64-71	Bidirectional three-state DATA bus. Used to transfer DATA between system bus and BPCRT2. Must be stable when UDSN or LDSN are asserted during write access. Driven by BPCRT2 during Read cycles.
UDSN	I	41	Upper Data Stobe. Active low. When asserted, UDSN indicates that data is being addressed on D0 to D7.
LDSN	I	40	Lower Data Stobe. Active low. When asserted, LDSN indicates that data is being addressed on D8 to D15.
R/WN	I	39	Read/Write. This input indicates the direction of tranfer on the system bus. When low, indicates Data is to be written into BPCRT2 controlled resources.
CSN	I	52	Chip Select. Active Low. Validates address decode for system access, must be low to access BPCRT2 controlled resources.
DTACKN	O	38	DATA Transfer Acknowledge signal. Active Low, open drain. Asserted by BPCRT2 when the system bus cycle can be continued.
RSTOUTN	O	35	RESET Output. Active Low, open drain. Asserted by the BPCRT2 Reset Sequencer during the reset procedure.
HALTN	O	36	HALT line Output.Active Low, open drain. Asserted by the BPCRT2 Reset Sequencer during the reset procedure.
BERRN	O	37	BUS ERROR Output. Active Low, open drain. Asserted by the BPCRT2 Watch-dog timer circuit if UDSN or LDSN are still asserted at the end of the time-out period.
CSROMN	O	54	Chip Select ROM Output. Active Low. Asserted by a Read access on the system bus in the ROM address area and when UDSN or/and LDSN are asserted.
CSI/ON	O	53	Chip Select I/O Output. Active Low. Asserted by a Read or Write access on the system bus in the External I/O area, and when UDSN or /and LDSN are asserted.
INTN	O	55	Interrupt request output. Active low, open drain. Used to generate interrupts to the CPU.

DYNAMIC RAM INTERFACE

MA0-MA8	I/O	10-3 120	Memory Address lines. Three state. Multiplexed ROW/COLUMN Address line outputs for DRAM control. Only MA0 to MA7 are significant when 64K DRAMs are used. Least significant bits for Address inputs (A1 to A9) from Coprocessor when CYACK output is asserted.
MD0-MD15	I/O	87-92 95-98 101-106	Bidirectional Memory Data bus. Three-state. Also Address and control input during coprocessor cycle.
RASN	O	117	Row Address Strobe. Active low. Valids the DRAM row address on the falling edge.
CAS1-4N	I/O	116-113	Column Address Strobes for memory Bank 1 to 4. Active Low. Valids the DRAM column address on the falling edge. During the reset period, Active High Valids Bank inputs. CAS4 is only used with 64K devices.
CSCGN	O	109	Chip Select Character ROM output. Active low. Used only with the coprocessor interface.
UWRN	O	119	Upper Write signal for DRAM. Active low. Is asserted when writing the most significant byte of the DRAM.
LWRN	O	118	Lower Write signal for DRAM. Active low. Is asserted when writing the least significant byte of the DRAM.
DTN	O	112	DATA transfer output. Active low. Used for Video DRAM devices.

CRT CONTROLLER INTERFACE

P0-P3	O	73-76	Pixel output in 4 bits per pixel mode. Output the 4 MSBs of the pixel in 8 bits per pixel mode.
P4-P7	O	80-83	Output the 4 MSBs of the pixel in 8 bit per pixel mode.
PCLK	O	78	Pixel Clock. Indicates P0-P7 (or P0-P3) lines are valid on the rising edge.
WRPN	O	72	Write Palette output. Active low. Indicates that data available on P0-P7 is control information. Used for an external palette or a Back-end chip.
VSYNC	I/O	85	Vertical Synchronisation. Active low, Three-state. In Master mode, this output is used as Vertical synchronisation signal for monitor. In Slave TV mode or in Slave Dual mode, becomes a vertical synchronisation Input.
HSYNC	I/O	86	Horizontal Synchronization. Active Low, Three-state. In Master mode or Slave TV mode, this output is used as horizontal synchronization signal. In Slave dual mode, it becomes an horizontal synchronisation Input.

CSYNCN	**O**	**57**	Composite synchronisation. Active Low, three-state. In Master mode, generates the composite synchronization signal. In Slave TV, generates a symetrical signal which has the horizontal frequency. In Slave Dual mode, generates the phase error between the master and the slave BPCRT2. When display is desabled, this input is used to initialize the synchronization mode.
BLANK	**O**	**84**	Blanking output. Active Low, three-state. Is asserted during vertical and horizontal blanking periods and high the rest of the time except when the Standard EBU is set. In this case and in the 30 MHZ mode, the screen border are in high impedance in order to allow the Standard EBU resolution.
DA	**O**	**58**	Display Active output. Active Low, three-state. Is asserted during the vertical retrace period, is in high impedance during the horizontal retrace period, and high the rest of the time.
M/SN	**I**	**60**	Master/ Slave input. When high, selects the Master mode.

COPROCESSOR INTERFACE

CYREQN	**I**	**107**	Cycle Request input from coprocessor. Active low. When asserted, it provokes an information transfer cycle for the coprocessor.
CYACKN	**O**	**111**	Cycle Acknowledge output for the coprocessor. Active Low. Is used for Handshake with the coprocessor.

MISCELLANEOUS SIGNALS

XTAL1	**I**	**123**	Crystal Oscillator Input. Can also be used for External clock Input.
XTAL2	**O**	**2**	Crystal Oscillator Output.
RSTINN	**I**	**59**	Reset input. Active low. Initiate a reset sequence . Internally pulled up.
XT/2	**O**	**122**	Xtal/2 Internal clock output. Frequency is Crystal frequency divided by 2.
XT/4	**O**	**121**	Xtal/4 Internal clock output. Frequency is Crystal frequency divided by 4.
TST	**I**	**61**	Test input. Active high. Must be grounded to VSS in normal condition.
IPA	**I**	**56**	Implicit Pixel accelerator Addressing. Active high. It can be used in order to have an implicit addressing of the pixel accelerator in order to increase the manipulation speed.
VDD (9)	**I**	**15-31-48-62 79-93-99-108-124**	Power supply pins (5 Volts).
VSS (9)	**I**	**1-17-32-46 63-77-94-100-110**	Power and signal GROUND pins.

FUNCTIONS

The BPCRT2 combines in one integrated circuit several functions necessary to implement a basic computer with a 68070 CPU and some memory devices.

The main available functions are:

-> **DISPLAY CONTROLLER** with on-chip timing chain, video address generator and shift register logic. A special reload mechanism permits the use of control words dynamically during the display.

-> **SPECIAL DISPLAY FILE DECODER** which permits the display of Run-Length coded files and performs the "MOSAIC" effect by using MOSAIC compressed files.

-> **SYSTEM CONTROLLER** logic integrating the necessary functions for a minimal system.

-> **DYNAMIC RAM CONTROLLER** with direct drive for several types of commonly available devices.

-> **PIXEL MANIPULATION LOGIC** optimized for image manipulation under CPU or Coprocessor control.

-> **COPROCESSOR INTERFACE** to be used with a high speed dedicated drawing/manipulation peripheral processor. Can also be used to obtain double access memory system.

DISPLAY CONTROL

The BPCRT2 contains the necessary logic to read sequentially the content of a memory area and to serialize it nibble per nibble or byte per byte. The BPCRT2 has a built-in timing generator to assure the generation of the necessary synchronisation signals for the various parts of the chip and for control of the monitor or TV set used as display unit. The device is programmable for several pre-defined modes of display in order to adapt to various applications.

RESOLUTIONS

BPCRT2 can display images using various modes. These modes are controlled by the DISPLAY COMMAND REGISTER (DCR).

Horizontal resolution:

The horizontal resolution is set by the following bits of the DCR :

CF1,CF2 : CLOCK FREQUENCY, 4 different frequencies are possible.
SS : SCREEN SIZE, this bit selects either a full size display (SS=1) for over scanned images or reduced display (SS=0) with an horizontal an vertical programmable color border.
CM : COLOR MODE, this bit sets the display to double resolution 4 bits per pixel (CM=1) or single resolution 8 bits per pixel (CM=0).

The following table gives the various possibilities:

CF1	CF2	SS	Frequency	Nb of Px/line CM=1	CM=0	Active line
0	0	0	19.6608*	448	224	45.6µS
0	0	1	19.6608*	512	256	52µS
0	1	0	24 MHz	512	256	42.6µS
0	1	1	24 MHz	640	320	53.3µS
1	0	0	27.5 MHz	640	320	46.5µS
1	0	1	27.5 MHz	720	360	52.4µS
1	1	0	30 MHz	640	320	42.6µS
1	1	1	30 MHz	768 +	384+	51.2µS

TABLE 1

NOTES:
* This frequency is used by the 68070 and allows for a single frequency minimal system.
+ The number of visible pixels can be reduced to 360 or 720 by utilizing the BLANKN signal to reduce the visible line to 48 µS (see VIDEO SYNCHRONIZATION).
-->If the NORMAL mode is used for DRAM access, ~~only the 4-bits/pxl mode is available and~~ the resolution is half.
-->In Double frequency mode (SM=0,DF=1), the line period and the horizontal resolution are divided by 2. This mode does not exist with CF1=CF2=0.
-->When using Dual Port Video Ram with external shift registers, it is possible to increase the resolution.

Vertical resolution:

The vertical resolution is set by the following bits in the DCR are :

FD : FRAME DURATION, this bit selects a 50 or a 60 Hz scan frequency (assuming the CF1-2 bits are set to an allowed crystal frequency in table 1). A zero forces a 50 Hz scan (312 or 625 lines per frame). When FD is set to 1, the scan becomes 60 Hz compatible (262 or 525 lines).

SS : SCREEN SIZE , as for the horizontal size, this bit has an effect on the vertical size of the active screen. If set to 1, the display will be compatible with a full screen display like TV image. When SS bit is reset to 0, the display becomes reduced with a top and a bottom border of the programmable color.

SM , DF : These 2 bits permit the use of 4 different scan modes as indicated as follows :

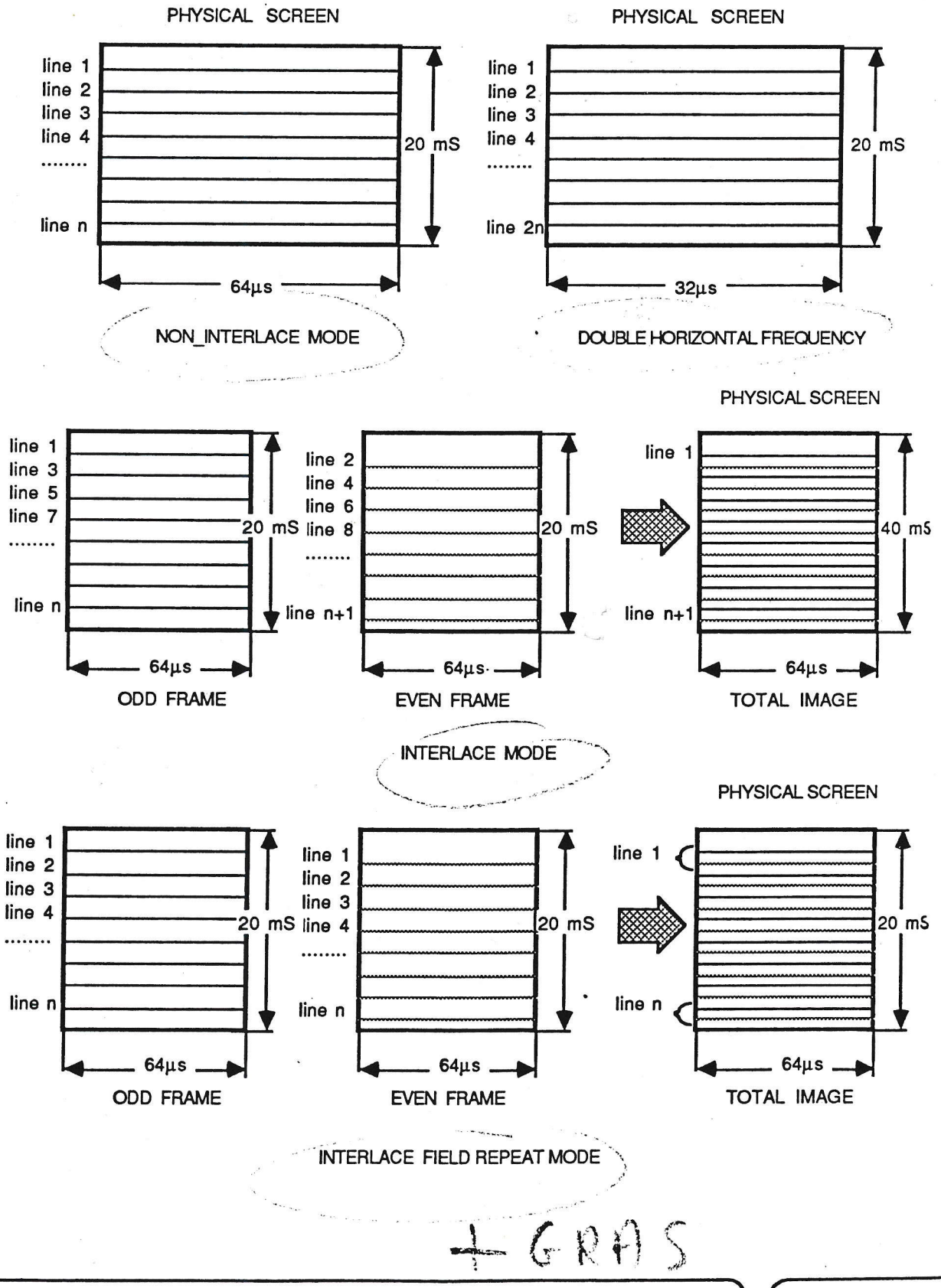
SM	DF	SCAN MODE
0	0	Non-interlace mode.
0	1	Non-interlace mode with a double horizontal frequency. The vertical frequency is the same, this doubles the vertical resolution. Not usable with CF1=CF2=0
1	0	Interlace mode. 2 interleaved frames are generated, the odd frame displays the odd memory lines and the even frame displays the even memory lines. At the end of the memory line N display, there is an automatic jump to the memory line N+2. The displayed memory size is 2 times bigger than in the non-interlace mode.
1	1	Interlace field repeat mode. This interlace mode has 2 interleaved frames displaying the same memory field. The displayed memory size is the same as in non-interlace mode. This permits synchronization with the TV standard.

The following table summarizes the various possibilities:

FD	SS	SM	DF	Nb of lines	Frame Duration	Image Frequency
0	0	0	0	250	16mS	50Hz
0	0	0	1	500	16mS	50Hz
0	0	1	0	500	16mS (x2)	25Hz
0	0	1	1	250	16mS (x2)	50Hz
0	1	0	0	280	18mS	50Hz
0	1	0	1	560	18mS	50Hz
0	1	1	0	560	18mS (x2)	25Hz
0	1	1	1	280	18mS (x2)	50Hz
1	0	0	0	210	13.4mS	60Hz
1	0	0	1	420	13.4mS	60Hz
1	0	1	0	420	13.4mS (x2)	30Hz
1	0	1	1	210	13.4mS (x2)	60Hz
1	1	0	0	240	15.3mS	60Hz
1	1	0	1	480	15.3mS	60Hz
1	1	1	0	480	15.3mS (x2)	30Hz
1	1	1	1	240	15.3mS (x2)	60Hz

TABLE 2

FIGURE 3: SCAN MODE, EXAMPLES OF SCREEN DISPLAYED (frame frequency=50Hz)



+ GRAS

DISPLAY MODES

Reduced and full screen

Two modes are available mainly intended either for TV applications where an over-scanned picture is used or for text applications where it is necessary to see the total active screen. The first mode is named Full-Screen mode (SS=1) and the second mode is named Reduced Screen mode (SS=0). In Reduced Screen mode, a border of programmable color is displayed on the top, bottom, left and right parts of the visible screen.The BORDER REGISTER is 8 bits wide allowing for 256 colors in 8 bits per pixel mode or for 16 colors in 4 bits per pixel mode. In this case, only the 4 MSBs are used (BORDER[7:4]).

Physical and logical screen

Independently of that, two types of memory arrangements are available. The simple case is named Physical Screen mode; it corresponds to a direct representation of an area in memory where the first pixel of a line is placed immediately after the last pixel of the previous line. The other, named Logical Screen mode uses a fixed length of a line in memory which is longer than the visible line. It allows rolling of the display horizontally.

The bit LS of the DCR is used to set one of these 2 modes.

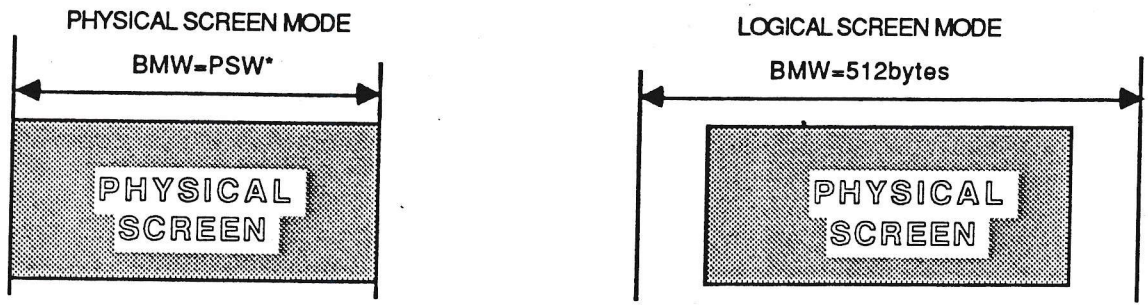
At the beginning of each frame the VIDEO START ADDRESS REGISTER (VSR) points to the first pixel of the first video line to be displayed. The pixels to be displayed at the other video lines depend on the type of screen.

--> In **Physical Screen** mode (LS=0), the first pixel address of the current video line (fpacl) is just after the last pixel address of the previous line (lpapl), that means: fpacl=lpapl+1.
When the scan mode is interlaced (SM=1,DF=0), fpacl=lpapl+1+1line.
When the Interleaved Dynamic Control Area DCA (see next chapter) is set, fpacl=lpapl+1+DCAsize.
When the interleaved DCA and interlace mode are set, fpacl=lpapl+1+1line+DCAsize.
It is not possible to use the reduced DCA mode and the interlace mode simultaneously. The physical screen mode permits to optimize the memory area and avoid refresh cycle during the display area.When using subscreens by reloading the VSR register, one of 2 consecutives subscreens must have at least 4 lines to insure the memory refresh. In the 27.5 Mhz mode and in full screen mode, the Physical Screen width is 768 pixels even if the resolution is 720 pixels in 4 bits per pixel mode (respectively 384 and 360 pixels in the 8 bits per pixel mode).

--> In **Logical Screen** mode (LS=1), the video lines (in memory) start at an address multiple of 128 long words. The physical display starts at the value of the Video Start Address register and ends after the programmed number of pixels per video line.
To fetch the first pixel of the current line, the LSBs of the Video Start Address register are reloaded into the counter and the MSB are incremented of 128 longwords. Thus fpacl=fpapl+128longword.
The width of the logical screen is equal to 512 bytes independently of the resolution chosen , so giving an area of 1024 pixels in 4bits/pxl mode or 512 pixels in 8bits/pxl mode. The displayed memory area is always less than 512 bytes, this gives the possibility of horizontal rolling.

WRAP AROUD

FIGURE 4: PHYSICAL and LOGICAL MODE



* BMW=Bit Map Width PSW= Physical screen Width

IMAGE CONTROL AREA (ICA) and DYNAMIC CONTROL AREA (DCA) MECHANISMS

The BPCRT2 offers the possibility to fetch control information during horizontal and vertical retrace periods in order to change the contents of internal registers, to control a Back-end processor (BEP) or to generate an interrupt. Two bits are used to control these mechanisms (IC and DC).

ICA mechanism

The image control area (ICA) mechanism consists of fetching instructions during the vertical retrace period.

In the begining of the vertical retrace period, BPCRT2 fetches the first ICA instruction at the location H400. or H80400 (see DRAM DESELECT) which is the beginning of the ICA. The ICA instructions can be passed to the BEP or used internally to reload the border color register or the video start address (VSR) or drive the interrupt pin. When an ICA STOP instruction is decoded, the VSR is reloaded for display and the BPCRT2 waits for the beginning of the active display area.

The size of the ICA can be large because the ICA fetches take place during the non-dispayed lines of the vertical retrace. This mechanism allows for reload of a 256 entry Colour Look-up Table (CLUT) in the BEP and complete update of the mode of the system during one frame retrace. The instruction "reload VSR" permits an indirect addressing which can be used to place the ICA anywhere in the first megabyte of memory.

DCA mechanism

The dynamic control area (DCA) mechanism has the same concept as the ICA mechanism but it is performed at the end of each video line, allowing dynamic control during an image display. The DCA is fetched immediately after the end of the active display line and not during the vertical retrace.The DCA has the same type of instructions as the ICA. The memory allocation for the DCA depends on which mode is set by the ID bit of the DCR2 register: The **Interleaved DCA** mode (ID=0)
The **Independant DCA** mode (ID=1)

Interleaved DCA mode

In Physical Screen mode, the DCA is placed between the end of the physical line and the beginning of the next line. The size of the DCA is either 16 Bytes (reduced DCA) or 64 Bytes.

In Logical Screen mode, the DCA is placed in the last part of the logical line. When the physical video line is fetched, the LSBs of the long word address are forced to 1F0 (reduced DCA) or 1C0 in order to fetch the first control word of the DCA. It is then incremented normally. The logical screen is wrapped between the long word just before the DCA and the first location of the line so the DCA will never be fetched as active display area if the VSR never points to the DCA area.

Independant DCA mode

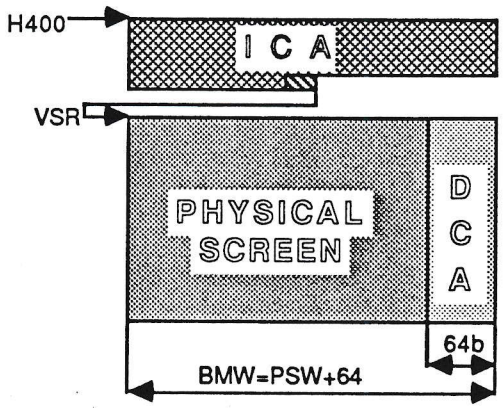
For this mode the DCA is an independant bitmap which is 16 bytes (reduced DCA) or 64 bytes wide. The first line is pointed to by a dedicated DCA POINTER, DCP, which is different from the VSR register that points to the display area and the ICA. DCP is longword aligned. The DCA of the second line is automatically pointed to by DCP+16 bytes (reduced DCA) or by DCP+64 bytes. As for the VSR register, it is possible to change the content of the DCP register during the display in order to use a different independant DCA bitmap.

In Physical Screen mode, the DCA size is not added to the physical line, the displayed memory lines are always adjacent.

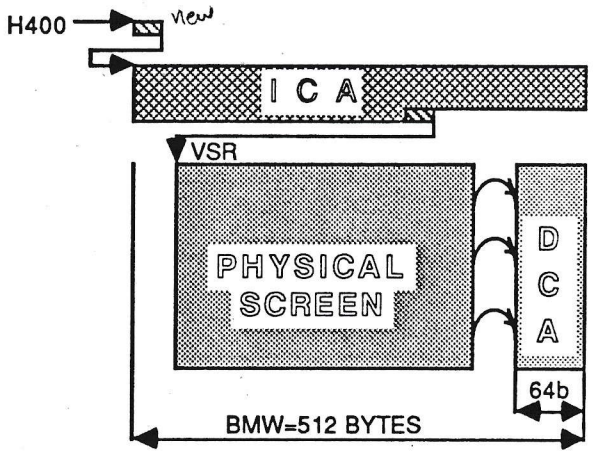
In Logical Screen mode, the logical screen is entirely dedicated for the display. The Logical line is wrapped between the first pixel and the last pixel of the line. It is therefore easier to perform horizontal rolling.

FIGURE 5: ICA and DCA examples

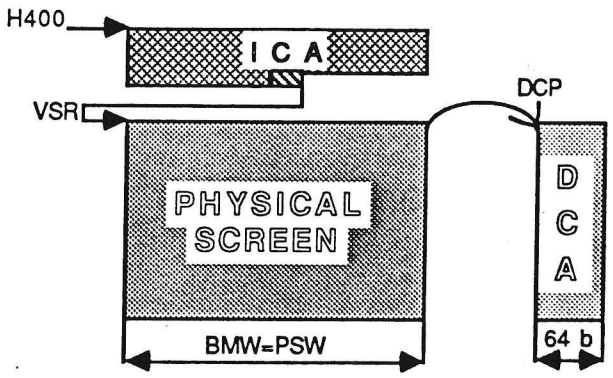
PHYSICAL SCREEN MODE WITH ICA AND INTERLEAVED DCA



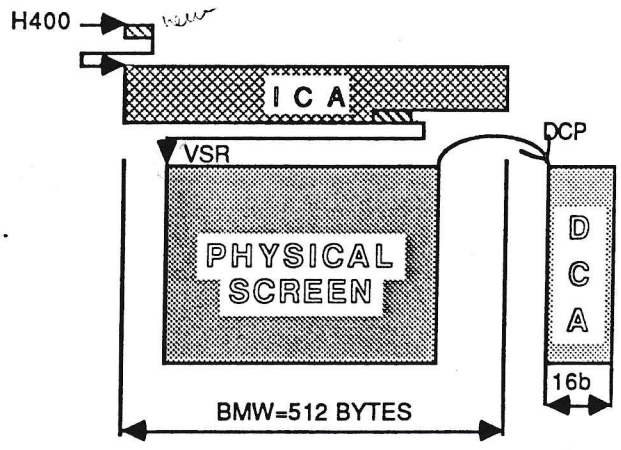
LOGICAL SCREEN MODE WITH ICA AND INTERLEAVED DCA WITH INDIRECT ADDRESSING OF THE ICA



PHYSICAL SCREEN MODE WITH ICA AND INDEPENDANT DCA



LOGICAL SCREEN MODE ICA WITH INDIRECT ADDRESSING OF THE ICA, INDEPENDANT AND REDUCED DCA



* BMW=Bit Map Width
PSW= Physical screen Width

▨ = "RELOAD VSR and STOP" INSTRUCTION

DCA and ICA Initialization

The control areas are set using the IC and DC bits of the DCR register. There are then four possible modes:

IC	DC	ICA	DCA	**TABLE 3**
0	0	no	no	
0	1	yes	yes --> REDUCED DCA MODE DCA size = 16 bytes	
1	0	yes	no	
1	1	yes	yes --> DCA size = 64 bytes	

When IC=DC=1, the number of possible fetches in the DCA can be limited by the line retrace duration. The following table indicates the different possibilities :

TABLE 4:

DOUBLE FREQUENCY (SM=0,DF=1)	SS	CF1	CF2	DCA in bytes
0	0	0	0	64
0	1	0	X	32
0	1	1	0	32
0	1	1	1	64
1	X	X	X	16

When the effective DCA is longer than indicated, an automatic STOP is performed.

The allocated memory size for the DCA is always 64 (IC=DC=1) or 16 bytes (IC=0,DC=1) even if the effective DCA size is shorter. In SLOW mode (for the DRAM), the possible DCA fetches are divided by 2.

ICA and DCA Instructions

An instruction is 32 bit wide and longword aligned, so always pairs of words will be fetched. The content of the MSBs of those long words give the operation to be performed. 9 different instructions are possible :

TABLE 5:

0000 ---- ---- ---- ---- ---- ---- ----	**STOP.** Stop the control sequence. The instructions fetches are then stopped for the rest of the line concerning the DCA or until the beginning of the active display area concerning the ICA.
0001 ---- ---- ---- ---- ---- ---- ----	**NOP.** No operation.
0010 ---- ---- PPPP PPPP PPPP PPPP PPPP	**RELOAD DCP.** Reload the DCP and its associated address counter with the specified pointer. The next fetches will use the new value. This permits an indirect addressing for the independant DCA mechanism.
0011 ---- ---- PPPP PPPP PPPP PPPP PPPP	**RELOAD DCP and STOP.** Reload the DCP with the specified pointer, then stop control fetches as with the STOP instruction.
0100 ---- ---- PPPP PPPP PPPP PPPP PPPP	**RELOAD VSR.** Reload the VSR and the video address counter with the specified pointer. The next fetches will use the new value. This permits the use of subscreens or indirect addressing for the ICA and the interleaved DCA.
0100 ---- ---- PPPP PPPP PPPP PPPP PPPP	**RELOAD VSR and STOP.** Reload the VSR with the specified pointer, then stop the control fetches as with the STOP instruction.
0110 ---- ---- ---- ---- ---- ---- ----	**INTERRUPT.** Generate an interrupt to the CPU.
0111 ---- CCCC CCCC ---- ---- ---- ----	**RELOAD BORDER.** Reload immediately the border color register with the specified color.
1XXX XXXX XXXX XXXX XXXX XXXX XXXX XXXX	**BEP CONTROL.** Control of the Back-End processor. (see BEP interface). The WRPN signal goes low and the 32 bits are passed to the BEP without alteration.

SCREEN MANAGEMENT

When the IC and DC bits are equal to zero (no Control Area), the start address of the screen must be loaded by the CPU in the video start register VSR before activation of the display controller. This register is 20 bits wide, so the screen start can be located anywhere in the first Mbyte of RAM(H0 to H100000).

Horizontal and vertical rolling

Because of the DRAM interface used, the beginning of each line is long word aligned. In logical screen mode, a horizontal offset can be introduced to allow for horizontal soft rolling pixel per pixel in 8 bits/pxl mode or 2 pixels per 2 pixels in 4bits/ pxl mode. In order to specify the offset to start with, 2 bits are added acting as LSBs of start address to define a byte address. Those bits are placed in the VSR as 00 and 01 locations, resulting in a 20-bit byte address pointing to an area in DRAM.

The ability to change the VSR value for the beginning of the frame allows vertical rolling line per line from one frame to the next one. The CPU will have to reload the VSR with current address plus or minus the width of the bitmap.

By reloading the VSR dynamically, the ICA and DCA mechanism make the horizontal and vertical rolling easier.

Subscreens

The reloading of VSR effects a "jump" from one memory location to another. This allows the display of several subscreens, each of them being built from a different memory area. Changing the various new VSR values in the DCAs will generate rolling or scrolling inside each subscreen independently.

PIXELS OUTPUT

The BPCRT2 gives two possible modes of pixel output by serializing the memory contents in two ways. The 16-bit words are divided either in 2 bytes to be serialized via 8 outputs (P0 to P7) or in four nibbles to be serialized via 4 outputs (P0-P3). The correspondance between displayed memory word and pixel is as follows:

In 4 bits per pixel:	P0 = D15-->D11-->D7-->D3		P1 = D14-->D10-->D6-->D2	
	P2 = D13-->D9-->D5-->D1		P3 = D12-->D8-->D4-->D0	
In 8 bits per pixel:	P0 = D15-->D7	P1 = D14-->D6	P2 = D13-->D5	P3 = D12-->D4
	P4 = D11-->D3	P5 = D10-->D2	P6 = D9-->D1	P7 = D8-->D0

The output of the pixel content is clocked by the Pixel Clock signal (PCLK). In 4bits/pxl mode, the PCLK frequency is the XTAL frequency divided by 2 (max: 15 MHz) , in 8bits/pxl mode it is XTAL frequency divided by 4 (max: 7.5MHz). On rising edges of PCLK, the data presented on P0-P7 (or P0-P3) is valid.

When the 4bits/pxl mode is selected, the P4 to P7 outputs are zeroed.

During the blanking period, the pixel content will be zero (if DC=0).

During the display period, the BPCRT2 transfers to the pixel output, the bytes (or nibbles) in a transparent way (no interpretation of the contents). It is possible to add a Back-End Processor which can perform additionnal pixel processing before transmission to the monitor.

When used without a Back-End processor, the BPCRT2 can generate 4 or 8 bits for a resistor network or a set of three D/A converters.

BACK-END PROCESSOR (BEP) INTERFACE

During the Horizontal retrace periods (including vertical retrace), the BPCRT2 can generate control signals for the BACK-END Processor if the Image Control or Dynamic Control Mode (IC or DC bit) are selected. The Write palette signal (WRPN) is asserted to indicate that the DATA available on P0-P7 (even in 4-bit mode) is not a pixel content but a value to be loaded into the Back-End Processor. This information is composed of a serie of up to 16 Longwords (64 transfers) coming from an ~~area written in memory by the CPU or Coprocessor~~. The various registers of the Back-End Processor can be reloaded before each video line using this mode.

The information will be sent to the Back-End Processor in groups of 4 bytes. The BPCRT2 will test the MSB (MD15) of the first word. If this bit is equal to one the transfer to the BACK-END processor will occcur. If MD12 to MD15 are zeroed, it will disable the control mode for the rest of the current video line. So it is possible to grant the remaining accesses to the coprocessor or to the system bus. Note that if the DC bit is set and if no control information is necessary for the current line, the user must reset the four MSBs of the first word of the DCA.

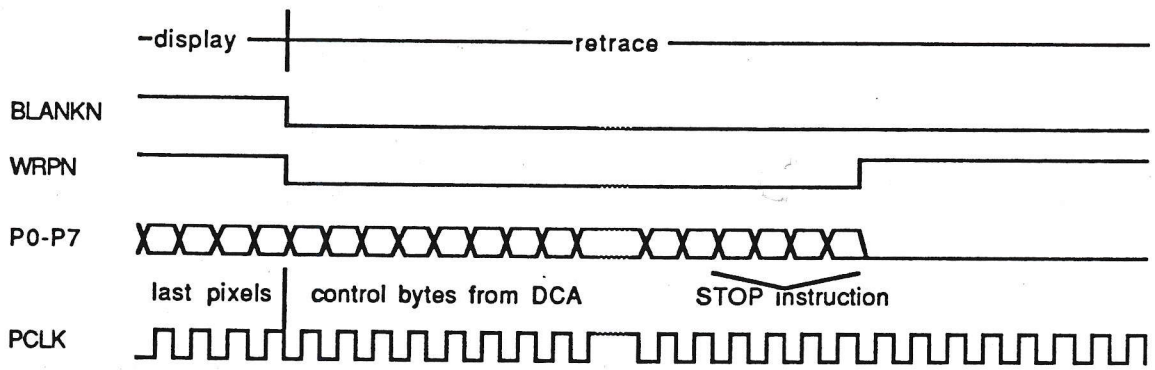
When the Reduced screen mode is performed, the border color is immediately sent to the back-end processor after the display active area. If the WRP signal is asserted when BLANK is still high, the BEP must hold the border color during the control sequence.

The BEP must stop the generation of the border color during the Blanking period.

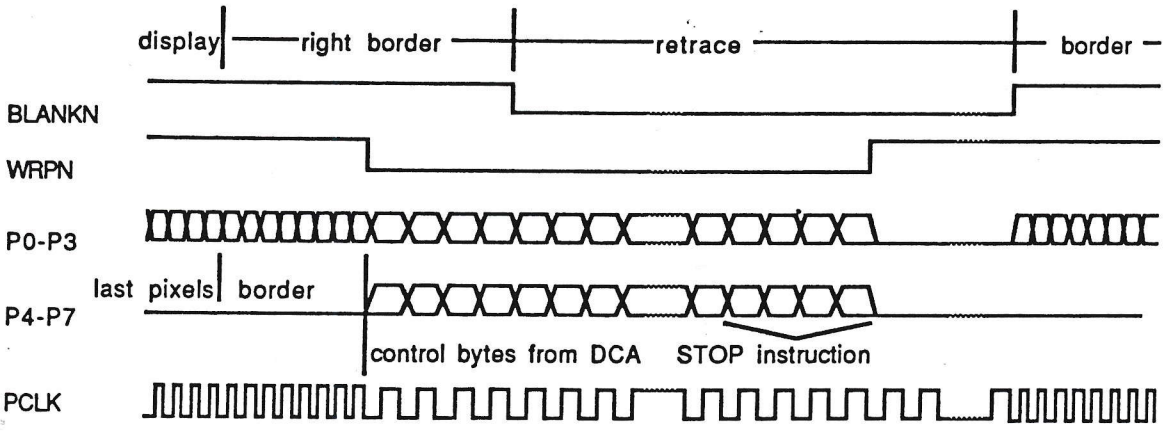
The following diagrams give the various sequences which can occur at the end of the active display lines:

FIGURE 6: BEP INTERFACE

8 bits/pixel full screen mode :



4 bits/pixel reduced screen mode :



VIDEO SYNCHRONIZATION

The BPCRT2 generates signals for synchronization of a TV set or a monitor. Furthermore, the synchronization signals are programmable to be a master, a slave to another BPCRT2 (DUAL MODE) or slave to incoming TV Synchronization signals. The status of the ~~MASTER~~/SLAVE and the ~~CSYNC~~ pins (when the DE bit of the DCR = 0) are used to set the synchronization mode as follows :

M/SN
CSYN

M/SN	CSYNCN pin DE=0	SYNCHRO MODE
1	X	MASTER
0	1	SLAVE TV
0	0	SLAVE DUAL

When DE = 0 (display disable), the CSYNCN pin is an input so that the SYNCHRO MODE can be initialized. A pull up resistor being internally connected to the CSYNCN pin, so the initialization of the slave TV mode does not need any pull-up resistor but a pull down resistor is necessary to initialize the slave dual mode.
When DE is set to 1, the CSYNCN state is latched and CSYNCN becomes an output pin .

If DE is zeroed the chip is in the display off mode, the synchro signals and the pixel output are in the high impedance state. The DRAM bus interface is still available for system and coprocessor accesses. DRAM access is not synchronized on video fetches anymore but are resynchronized on a host or coprocessor access to give a shorter reaction time and a better transparency for the host and/or coprocessor access. The DE bit is reset by the RESET sequence, and when it is set to 1, the synchro pins are used as follows:

In **MASTER** mode , HSYNCN, CSYNCN and VSYNCN signals are generated.

In **SLAVE TV** mode , HSYNCN is generated , the VSYNCN pin is in input mode and must receive an external VSYNC signal , the CSYNCN pin is used to output a signal which has the HSYNCN period but with a duty cycle = 1 to input into the phase comparator of an external phase-locked-loop oscillator. This signal is high during the first half of each line.

In **SLAVEDUAL** mode , HSYNCN and VSYNCN pin are in Input mode and have to receive external HSYNC and VSYNCN . CSYNCN generates the phase error between the internal and the external HSYNCN signal. This mode is used when more than one BPCRT2 are needed to increase the pixel depth, one is in MASTER or SLAVE TV mode, the others in SLAVEDUAL mode and receiving the synchro signals from the MASTER BPCRT2 .

The BLANKN information is active low during non display periods. The pin is driven high during the active display period. In the 30 MHz mode when the ST bit of the CSR is high, the BLANKN signal is in high impedance during the 12 first and 12 last pixels of the line in 8bits/pxl mode (24 pixels in 4bits/pxl mode). The Back-End Processor can thus display 384 or 360 pixels of 8 bits (768 or 720 pixels of 4 bits) with a pull-up or a pull-down resistor on the BLANKN pin.

The DA pin generates the Display Active signal which is low during the vertical retrace, high during the display line and high impedance during the line retrace. With a pull-up or pull-down resistor it is possible to disable or enable, respectively, the horizontal component of DA.

FIGURE 7 and TABLE 6 represent the horizontal timing with HSYNCN and the horizontal components of BLANKN and DA signal in Reduced screen mode. The timings available in the chart are given as an equivalent number of pixels per line when the 4 bits/pixel mode is used. It has to be divided by two in 8 bits/pixel mode and in DOUBLE FREQUENCY modes.

FIGURE 8 and TABLE 7 represent the vertical timing with VSYNCN and the vertical components of BLANKN and DA signal in Reduced screen mode. The timings given assume one line=64µS. In DOUBLE FREQUENCY mode the vertical timing is the same as in the non-interlace mode.

FIGURE 7:

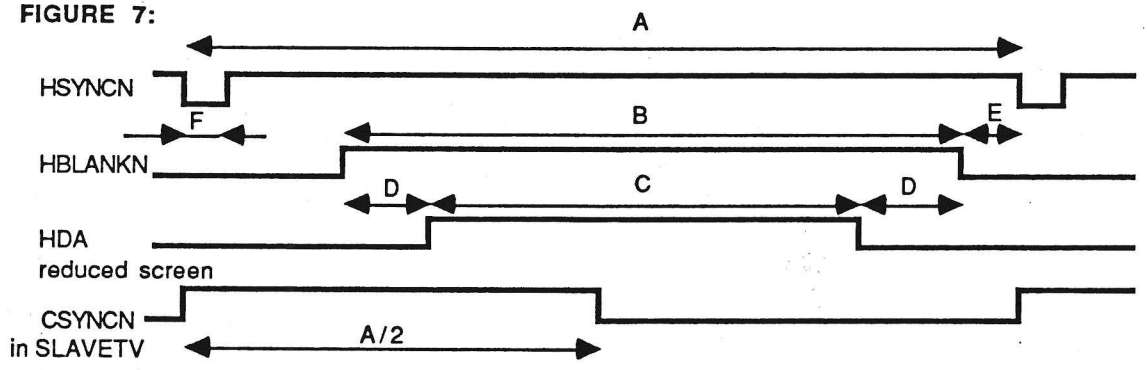


TABLE 6

	19.6608 Mhz		24 Mhz		27.5 Mhz		30 Mhz	
	Pixels	µS	Pixels	µS	Pixels	µS	Pixels	µS
A	640	65.1	768	64	880	64	960	64
B	512	52.08	640	53.33	720	52.36	768	51.2
C	448	45.57	512	42.67	640	46.55	640	42.67
D	32	3.26	64	5.33	40	2.91	64	4.27
E	16	1.63	8	0.67	16	1.16	24	1.6
F	48	4.88	56	4.67	64	4.65	72	4.8
G	24	2.44	24	2	32	2.33	32	2.13
H	48	4.88	56	4.67	64	4.65	72	4.8

FIGURE 8:

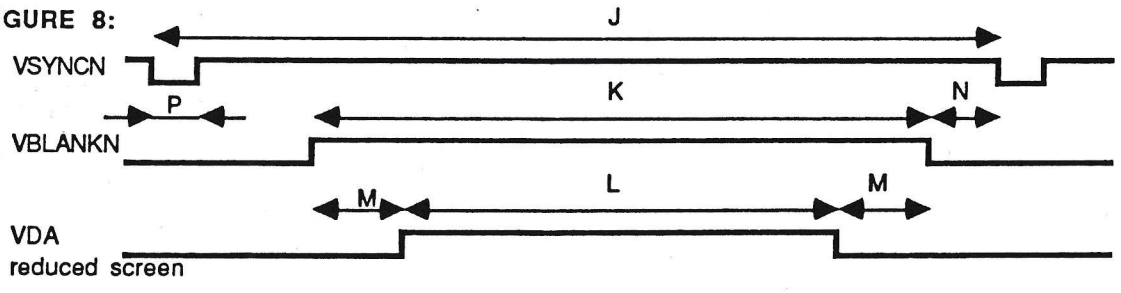


TABLE 7

	50 Hz non-interlace		50 Hz interlace		60 Hz non-interlace		60 Hz interlace	
	lines	mS	lines	mS	lines	mS	lines	mS
J	312	19.97	312.5	20	262	16.77	262.5	16.8
K	280	17.92	280	17.92	240	15.36	240	15.36
L	250	16	250	16	210	13.44	210	13.44
M	15	0.96	15	0.96	15	0.96	15	0.96
N	6	0.384	6 or 6.5	0.416	4	0.256	4 or 4.5	0.288
P	2.5	0.16	2.5	0.16	3	0.192	3	0.192

FIGURE 9 and 10 represent the CSYNCN signal when BPCRT2 is in MASTER mode and interlace mode (SM=1). The 50Hz mode is shown in figure 9 and the 60Hz mode is shown in figure 10.

FIGURE 9: CSYNCN in the 50 Hz mode

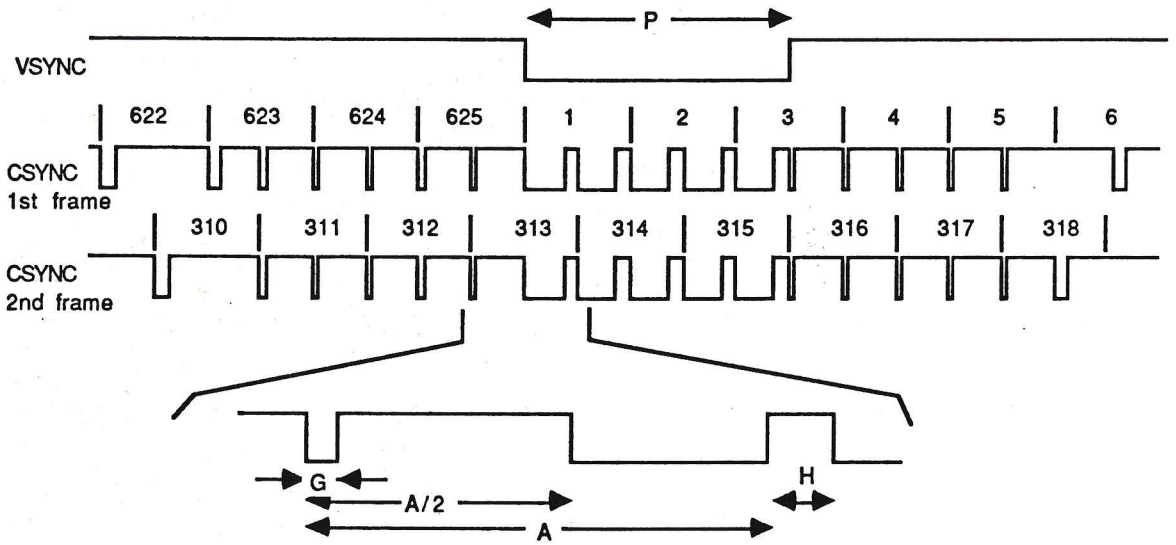
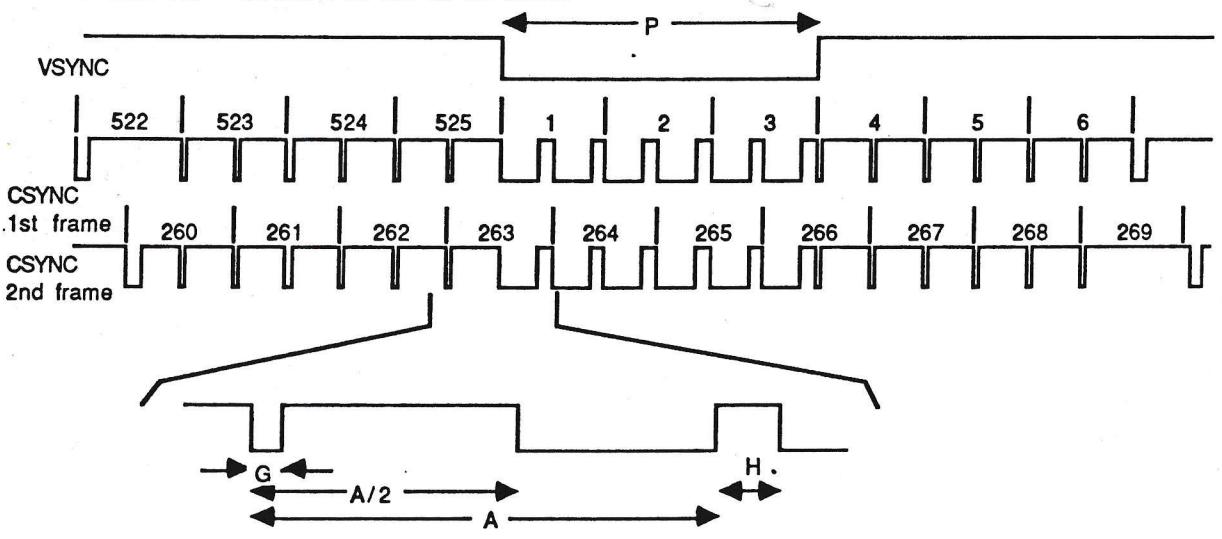


FIGURE 10: CSYNCN in the 60 Hz mode



FRAME GRABBING

The BPCRT2 can be synchronized on an incoming TV signal, which makes it possible (with a small amount of external circuits), to "grab" the image information and load it into the memory. When the FRAME-GRABBING bit FG is set, the BPCRT2 will end the current frame (two fields eventually) and start the grabbing period which is one or two frames long depending on the scanning mode.

During the grabbing period, the display scanning remains exactly the same but the UWRN and LWRN signals to the memory are asserted during the normal display active period. The external hardware must place the results of the A/D conversions for each pixel on the DATA bus, synchronously with the access to the memory. The memory will thus load the new picture and the BPCRT2 will display it as normal.

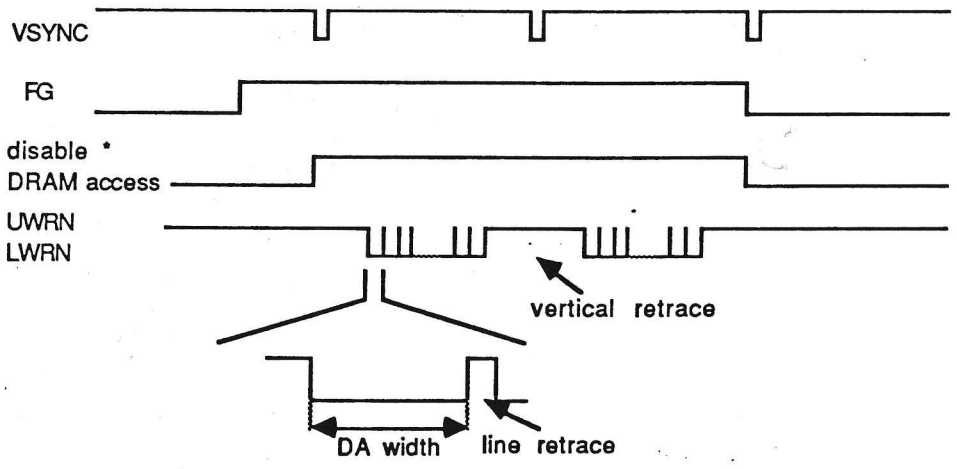
CPU or coprocessor memory access is not granted during the grabbing. The BERR generator is also disabled during the grabbing period. The internal registers are always accessible.

At the end of the frame grabbing, the FG bit is reset by BPCRT2 automatically and the previous mode is performed. During the grabbing the FG bit is readable in the command status register CSR.

The device is able to grab in real time, on-the-fly, TV images with a resolution of 768x560 pixels of 4 bits or 384x280 pixels of 8 bits.

FIGURE 11 shows a grabbing period in the interlace mode. During the 2 frames, the DRAM access is disabled and the DRAM write signals are asserted:

FIGURE 11: FRAME GRABBING



* internal signal

DISPLAY FILES

BPCRT2 can handle 3 types of file :

--> NORMAL file: organized as a bit map where each pixel has its own address
--> RUN-LENGTH file: consecutive pixels with the same color are grouped in the same block of information
--> MOSAIC file: as normal file but with resolution divided by a MOSAIC factor, the BPCRT2 is responsible for duplicating each pixel following the MOSAIC factor (2, 4, 8 or 16).

The 2 last types of files permit information compression to save space in the storage system, they are well adapted to achieve fast speed loading and animation.

The initialization of the file type is made with the FT1-2 bits of the DCR2 registers :

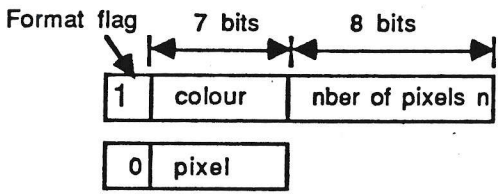
FT1	FT2	
0	X	NORMAL file
1	0	R-L file
1	1	MOSAIC file

RUN LENGTH

The RUN-LENGTH coding technique permits file compression by grouping in one block consecutive pixels which have the same color. The compression factor can be very important, for instance a screen which has a uniform colour needs a very short memory space in a RUN-LENGTH format. The RUN-LENGTH compression is applied to each video line independently of the others.

The RUN-LENGTH file is organized as a list of information about pixels without notion of width and height as in bit map files. The information indicates either the pixel colour followed by the number of consecutive pixels having the same colour, or the simple pixel. Thus, 2 formats are possible :

FIGURE 12:



The MSB indicates if the information is on 2 bytes (consecutive pixels having the same colour) or on 1 byte (pixel alone). The number of colours in 8 bits/pixel mode is therefore limited to 128. The number of consecutive pixels, n, is between 2 and 256. When n = 0, the display controller of BPCRT2 finishes the display line with the last indicated colour. Each line has to be finished with n = 0.
example :

Display =	Line 1 : blue	blue	cyan	grey	grey	grey	red	red	green	green	green
	Line 2 : pink	pink	pink	pink	pink	black	pink	pink	pink	pink	pink

File = blue 2 cyan grey 3 red 2 green 0 pink 5 black pink 0

In 4 bits/pixel mode, it is also possible to use the RUN-LENGTH technique. As BPCRT2 processes RUN-LENGTH files at the byte level, the RUN-LENGTH decoding works by groups of 2 pixels, each pixel being limited to 8 colours in order to use the MSB as a format flag. This format flag is output with the pixel of 3 bits via the pixel output port (P0-->P3).

example :

8 bits

|<-------->|

Display = red red red red blue blue blue pink pink pink pink pink → end of line

File = (red red) 2 (blue blue) (blue pink) (pink pink) 0

MOSAIC

The MOSAIC technique consists of changing the resolution of the screen by duplicating pixels and lines by a MOSAIC factor.
The effect on the screen is a granulation. The MOSAIC file can be compressed by a factor n x m where n is the horizontal MOSAIC factor and m the vertical MOSAIC factor.
Depending on the horizontal MOSAIC factor, BPCRT2 duplicates automatically the pixel on the line (horizontal MOSAIC). The MOSAIC factor is indicated into the DCR2 register :

MF1	MF2	MOSAIC FACTOR
0	0	2
0	1	4
1	0	8
1	1	16

example with horizontal MOSAIC factor = 2 and normal resolution = 10 pixels/line :

MOSAIC file = Green blue red orange brown yellow...

screen = line n°1 : Green green blue blue red red orange orange brown brown
line n°2: Yellow Yellow....

Concerning the vertical MOSAIC, the independant DCA can be used to duplicate the lines. The vertical MOSAIC can therefore be independent of the horizontal MOSAIC factor.

DCA AND INTERLACE MODE FOR RUN-LENGTH AND MOSAIC FILES

The video start register VSR is used to point at the beginning of lines as for the normal type of file. When using the DCA mechanism, only the independant DCA can be used, The concept of physical and logical screen does not exist anymore.
The interlace mode is not usable with RUN-LENGTH and MOSAIC files but it is possible to obtain the interlace effect with RUN-LENGTH files by using the interlace field repeat mode. In this case the VSR has to be changed at the end of each frame. The parity bit of the CSR status register indicates the frame parity for the interlace and interlace repeat mode. This bit permits synchronization of the reload of VSR with the 2 frames.

SYSTEM CONTROL

The BPCRT2 performs several system oriented control functions which are always necessary in a minimal system. The address decode, the access arbitration between various masters of the DRAM bus and the Reset timing generation are some of them. The following paragraphs will describe in detail the various functions.

ADDRESS DECODING

The BPCRT2 is connected to the system bus via 20 Address lines, giving 2 Megabytes of addressing range, the control bus (CSN, UDSN, LDSN, R/WN, DTACKN, BERRN, HALTN, RSTOUTN) and the 16-bit DATA bus. The chip controls the access to the resources of a minimal system i.e. 1.5MByte of DRAM, 0.5 MByte of ROM and internal registers and external I/O devices.

The system bus interface is 68000 compatible and is enabled when CSN is low and either UDSN or LDSN are asserted. The mapping depends on the type of DRAM which is used (256K or 64K) and on the synchro mode as indicated in this BPCRT2 mapping table :

TABLE 8

	256 K		64 K	
ADDRESS	MASTER OR SLAVE TV	SLAVE DUAL	MASTER OR SLAVE TV	SLAVE DUAL
000000 01FFFF	BANK 1	BANK 1	BANK 1	
020000 03FFFF			BANK 2	
040000 05FFFF			BANK 3	
060000 07FFFF			BANK 4	
080000 09FFFF	BANK 2	BANK 2		BANK 1
0A0000 0BFFFF				BANK 2
0C0000 0DFFFF				BANK 3
0E0000 0FFFFF				BANK 4
100000 17FFFF	BANK 3	BANK 3		
180000 1FFBFF	SYSTEM ROM		SYSTEM ROM	
1FFC00 1FFF7F	SYSTEM I/O	SYSTEM I/O	SYSTEM I/O	SYSTEM I/O
1FFF80 1FFFBF	DRAM I/O		DRAM I/O	
1FFFC0 1FFFDF		INT REGISTERS		INT REGISTERS
1FFFE0 1FFFFF	INT REGISTERS		INT REGISTERS	

Each BANK corresponds to a DRAM area and is associated with a CAS pin (CASN1-->CASN4).

The CSROMN pin is asserted when the SYSTEM ROM is decoded. During the 4 first CPU accesses the ROM shadowing technique places the ROM area in address 0 (see MEMORY SWAPPING).

BPCRT2 considers 2 types of external I/O :

The SYSTEM I/O for devices normally connected to the system bus

The DRAM I/O for devices hooked on the DRAM bus MD. If the address corresponds to these locations, the BPCRT2 will be transparent on address and data bus as for DRAM accesses.

In each case the CSION pin is asserted but the DTACK is generated only for the DRAMI/O (see DTACK generation).

The internal registers do not have the same mapping in SLAVE and MASTER modes to allow for independent access to 2 BPCRT2 with the same Chip Select.

In MASTER mode, TABLE 9 indicates the internal register map.

TABLE 9:

1FFFE0	CSR	Control/Status Register	Word Access
1FFFE2	DCR	Display Control Register	Word Access
1FFFE4	VSR	Video Scan Start Register	Word Access
1FFFE7	BCR	Border Color Register	Byte Access
1FFFE8	DCR2	Display Control Register 2	Word Access
1FFFEA	DCP	DCA pointer	Word Access
1FFFEC	SWM	PIXAC Selective Write Mask Register	Byte Access
1FFFEF	STM	PIXAC Selective Test Mask Register	ByteAccess
1FFFF0	A	PIXAC SOURCE Register	Word Access
1FFFF2	B	PIXAC DESTINATION Register	Word Access
1FFFF4	PCR	PIXAC COMMAND Register	Word Access
1FFFF7	MASK	PIXAC MASK Register	Byte Access
1FFFF8	SHIFT	PIXAC SHIFT Register	Byte Access
1FFFFB	INDEX	PIXAC INDEX Register	Byte Access
1FFFFC	FC	PIXAC Foreground COLOR Register	Byte Access
1FFFFD	BC	PIXAC Background COLOR Register	Byte Access
1FFFFE	TC	PIXAC Transparent COLOR Register	Byte Access

ACCESS ARBITRATION

The DRAM bus can be used by several masters on a cycle per cycle basis. An arbitration scheme is implemented to provide each master with a guaranteed access time. The various masters are:

- The system bus (CPU or DMA cycles)
- The display generator
- The refresh controller
- The optional drawing/manipulation coprocessor

The bus access is given with the following decreasing priority: Display generator, Refresh controller, and finally the system bus and the coprocessor which have the same priority.

When the display controller is active, the time is divided into slots of 16 clock periods (533 to 800 nS depending on the clock frequency) during which there is one window for the display controller and one for the system bus or the coprocessor. The display processor has always the first priority during the display window including during retrace if extra fetches are necessary for Image or Dynamic Control (if IC or DC bit =1). The system bus (CPU or DMA) and the coprocessor share the priority for the second window.

During the non display periods, the refresh controller has the first priority, the rest of time is for the system bus or the coprocessor. In order to limit the amout of wait states when the CPU or the Coprocessor access the memory, the sequence for DRAM access is resyncronized on the incoming requests.

The system bus and the coprocessor can use windows which are not used by the other one. The system bus can for example avoid access to the DRAM if the drawing command given to the coprocessor is time critical.

Access to the System ROM (decoded and acknowledged by BPCRT2) is possible independently of this arbitration because it does not require access to the DRAM bus.

The PIXel ACceleration logic, being accessible from system bus and from DRAM bus, is a common memory mapped resource, , and so requires an arbitration when accessed. Nevertheless, no synchronization will be necessary when accessed from the system bus.

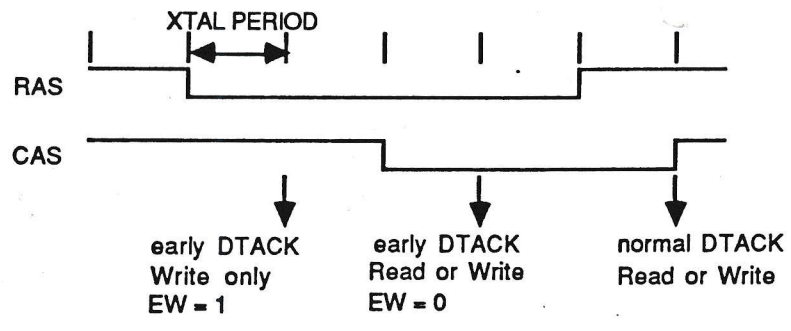
DTACK GENERATION

When a master of the system bus accesses the resources controlled by BPCRT2, the device will generate the acknowledge signal to allow the master to proceed. The access being synchronized on an available window, it may have to be delayed. Several modes are possible:

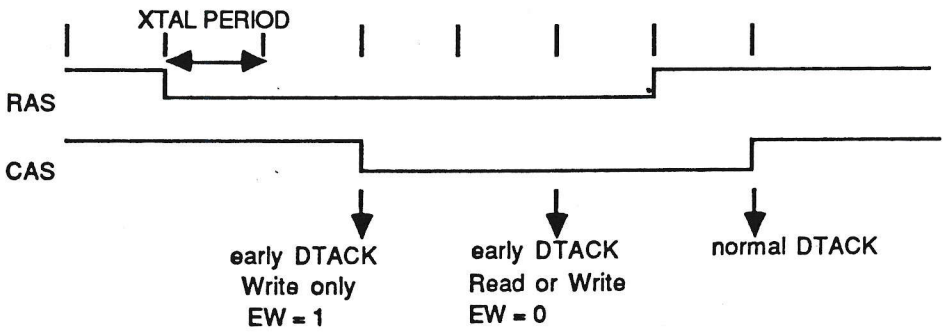
- The access to the DRAM will be acknowledged as soon as it is certain that the DATA will be available for the CPU. In order to shorten the bus cycle, DTACK can be asserted before the DATA is effectively valid (Early DTACK). If the ED bit in the CSR is equal to zero, a normal DTACK will be generated when the Data is valid on the system bus. If the ED bit is set, DTACK will be generated even two time slots before the early DTACK (66nS at 30 MHz) to speed up the CPU (or DMA for 68070). For a Write cycle, the DTACK can be generated 2 slots before if the bit Early Write EW, is set in the DCR register. The DTACK for a write can be advanced because the Address Strobe signal of the 680XX is not used by the BPCRT2. The following figure indicates the assertion time of the DTACK signal in the CPU window.

FIGURE 13:

DTACK assertion in FAST mode timing



DTACK assertion in SLOW mode timing



- Access to the internal registers will be acknowledged immediately after arbitration against a potential access from the coprocessor.

- Access to the System ROM will be acknowledged after a programmable delay counted from the internal timing chain (5 possibilities depending on the DD, DD1and DD2 bits of the CSR).

- The SYSTEM I/O device selection (CSI/O pin) is not acknowledged by the BPCRT2 but by the addressed device.

- The DRAM I/O are acknowledged as for the DRAM acknowledge , this device being considered completely synchronous with the access on the memory data bus MD.

BUS ERROR GENERATION

The BPCRT2 has a watch-dog timer function able to generate a BUS ERROR condition for the 68070. It is active when the BE bit of the Control register CSR is set to 1. When a resource is addressed on the system bus, (even if not controlled by the BPCRT2) by the assertion of UDSN or LDSN, the watch dog is incremented every video line . If the selection stays not acknowledged during two lines (64 to 128 µS), the BERR signal is asserted to finish the current bus cycle and the BE FLAG bit is set in the CSR. The CPU will then enter a BUS ERROR exception routine which must test this status bit. The Read Status Register instruction will automatically reset the BERR FLAG and the BERRN pin.

The BERR pin of the BPCRT2 is an Open Drain buffer with an internal pull-up resistor.

RESET AND HALT GENERATION

The BPCRT2 has a Reset input pin RSTINN, a Reset output pin RSTOUTN and a Halt output pin HALTN.

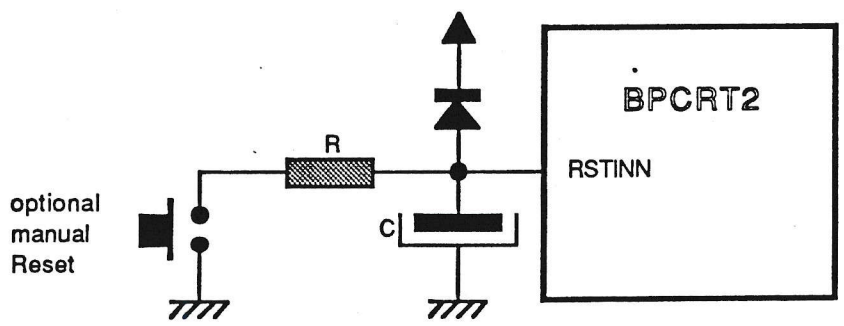
The Reset input is intended to be connected to a capacitor which will generate a low voltage at the begining of the Power-up period. It is detected and used to reset a Flip-Flop. When the on-chip crystal oscillator starts, the timing chain counts 8 frames and then clocks the Flip flop which releases the RSTOUTN pin. The HALTN pin is released one half line later. BPCRT2 is in the 20MHZ after activation of the Reset input pin, so delays on RSTOUTN and HALTN are compatible with a 680XX CPU whatever the XTAL frequency.

If a low voltage is applied again to the RSTINN input pin, the Flip-Flop will be reset, resetting the chip and provoking a complete new RESET sequence.

The RSTOUTN and HALTN pins of the BPCRT2 are Open Drain buffers with an internal pull-up resistor.

The diagram shows the basic reset circuit which is usable to reset the BPCRT2 and, via it, the rest of the system.

FIGURE 14: RESET CIRCUIT



X

MEMORY SWAPPING

The 68070, like the 68000 has its vector table in the first kilobyte of memory starting from address zero. The RESET mechanism consists of fetching the Supervisor Stack Pointer and the initial Program counter in the first four words of the same area. It is often required that the Operating System is able to manipulate the Vector table contents to update or to dedicate a configuration.

The BPCRT2 has a built in swapping mechanism to allow for this feature.

When reset, the first four accesses (SSP and PC) will provoke the selection of the ROM area (CSN must be asserted). The ROM content will be routed to the processor (Address=H0 for SSP and Address=H4 for PC). After this sequence, the DRAM and the ROM will be decoded normally.

The user must for this purpose place the relevant values of the initial SSP and the initial PC at the beginning of the System ROM area (H180000).

INTERRUPT GENERATION

The BPCRT2 can generate interrupts to the 68070 by asserting its INTN pin. This signal is intended to be routed to the INT1N or INT2N pin of the 68070 which uses a level sensitive without acknowledgment.

Each time the INTN signal is asserted, it generates an interrupt (of programmable level) in the 68070. The INTN pin is negated when the CPU reads the CSR status register.

Two conditions are able to generate an interrupt:

> The DCA mechanism can fetch an Interrupt instruction. This will set the IT1 bit in the CSR status register and assert the INTN pin. This mechanism allows for generating an interrupt every frame to synchronise the CPU operations.

> The PIXAC interface is declared free by the coprocessor (see PIXAC control registers). It will set the IT2 bit in the status register and assert the INTN pin. When the CPU read the CSR status register, the INTN signal is negated but the IT2 bit of the CSR remains high until the Pixel Accelerator is effectively used.

With the EN1 and EN2 bits of the CSR command register it is possible to ~~disable~~ avoid the propagation the INTN pin for the respective IT1 and IT2 bits.

DRAM INTERFACE

The BPCRT2 has an on-chip Dynamic RAM control and drive circuit programmable for various types of currently available memory devices.

DRIVING MODES

The BPCRT2 can drive directly up to 16 memory devices. It is possible to arrange them in one bank of 16 devices or in several banks of four devices.

Three or four CAS signals are available for the various banks.

The TYPE of DRAM (TD) bit in the Control/Status Register sets the DRAM interface for either 256K DRAMs or 64K DRAMs. In the first case, 9 multiplexed Address lines are generated and three CASN signals each select a bank of 512 KBytes.

In the second case, only 8 Address lines are available and the address decoding scheme is different. The fourth CASN signal is then available. In that mode it is possible to use one to four banks of four 64Kx4 devices.

The UWRN and LWRN signals control half of each bank to allow for instructions at the byte level.

When more than 16 devices are to be connected, external buffers must be used on MA0-8, UWRN, LWRN, CASxN and RASN signals.

When the coprocessor requires an access to the DRAM, the timing is still generated by the BPCRT2. The address is first transferred to BPCRT2 prior the RASN/CASxN sequence. The coprocessor then uses the DATA bus only (see COPROCESSOR INTERFACE).

DRAM TIMING

The Dynamic RAM interface timing is generated from the internal clock frequency produced from the on-chip oscillator. The basic cycle is a series of 16 time-slots, one time slot being a XTAL period.

During the display period, the ICA/DCA period and the refresh period, the basic cycle is divided in two parts, one window for the access of the internal address generator and one for the access of CPU or coprocessor. When using Dual-Port VRAMs, the 2 windows are for the CPU or the coprocessor during the display period, except for the first display cycle of each line, this cycle being used to reload the internal shift registers of the VRAM.

During non-display period, non-ICA/DCA period and non refresh period, the first window does not exist anymore, and the other window is triggered only when there is a CPU or coprocessor request.

The RASN/CASN timing is generated by using the 16 slots and resynchronizing with the internal clock before driving the buffers.

Two different timings are possible requiring different speeds of the DRAM devices:

--> The FAST mode is optimized for NIBBLE mode DRAM devices with an access time of 120 nS at 27.5MHz clock. The FAST mode also permits the use of PAGE mode DRAM devices. The FAST mode timing allows to access 2 consecutive 16-bit words using 9 slots. The remaining 7 slots are used to generate an access for the CPU or the Coprocessor. This FAST mode is also necessary when using double resolution images. The RAS is always generated in this case even if there is no CPU or coprocessor request.

--> The SLOW mode is based on two normal (single) accesses each using 8 slots. Only one 16-bit word is read for the display controller part which is enough for the single resolution and 4 bits per pixel. The speed of the DRAM devices can be lower in this case. Dual port Video RAMs are also driven using this mode. No RASN and CASxN are generated for the CPU window if there is no access request from the CPU or the coprocessor.

Different addressing schemes and slightly different timings are generated to drive the Nibble mode, the Page mode or the Dual ported Video Ram devices. Two bits of the Control/Status Register (DM1-2) can be set accordingly to the type of device effectively used:

DM1	DM2	TIMING SPEED	DRAM SUPPORTED
0	0	SLOW	NORMAL MODE
0	1	FAST	PAGE MODE
1	0	FAST	NIBBLE MODE
1	1	SLOW	DUAL PORT VIDEORAM

The correspondance between Memory Address bus MA and CPU Address bus A is as follows:

TABLE 10

	MA0	MA1	MA2	MA3	MA4	MA5	MA6	MA7	MA8
RASN	π	A2	A3	A4	A5	A6	A7	A8	μ
CASN	β	A11	A12	A13	A14	A15	A16	∂	Ω

$\pi = \begin{cases} A1 & \text{NORMAL OR NIBBLE MODE} \\ A10 & \text{PAGE MODE} \end{cases}$ $\beta = \begin{cases} A10 & \text{NORMAL OR NIBBLE MODE} \\ A1 & \text{PAGE MODE} \end{cases}$

$\partial = \begin{cases} A9 & 64K \\ A17 & 256K \end{cases}$ $\mu = \begin{cases} 0 & 64K \\ A9 & 256K \end{cases}$ $\Omega = \begin{cases} 0 & 64K \\ A18 & 256K \end{cases}$

The DUAL PORT mode has the same MA configuration as the NORMAL mode but the addresses valid on RAS are valid on CAS, and vice versa. For the NIBBLE mode DRAMs MA0 and MA8 have to be crossed externally.

FIGURE 15 shows the window timing in the **FAST mode**. The first window is a display window followed by a CPU read cycle then by a CPU write cycle. In the display window the column 2 is not generated for the NIBBLE mode DRAM but is automatically generated for the PAGE mode DRAM.

FIGURE 15:

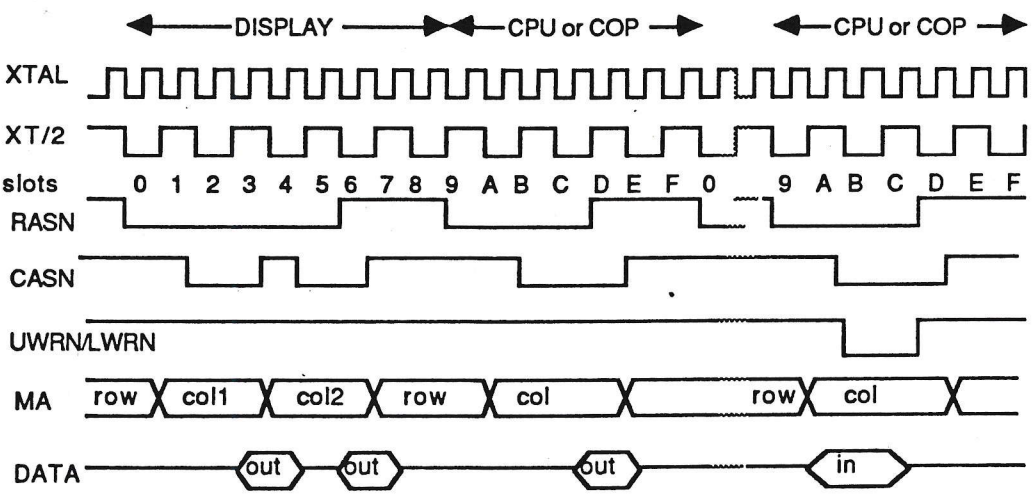


FIGURE 16 represents display and CPU windows in **SLOW mode**. The CPU (or coprocessor) access is a read cycle.

FIGURE 16:

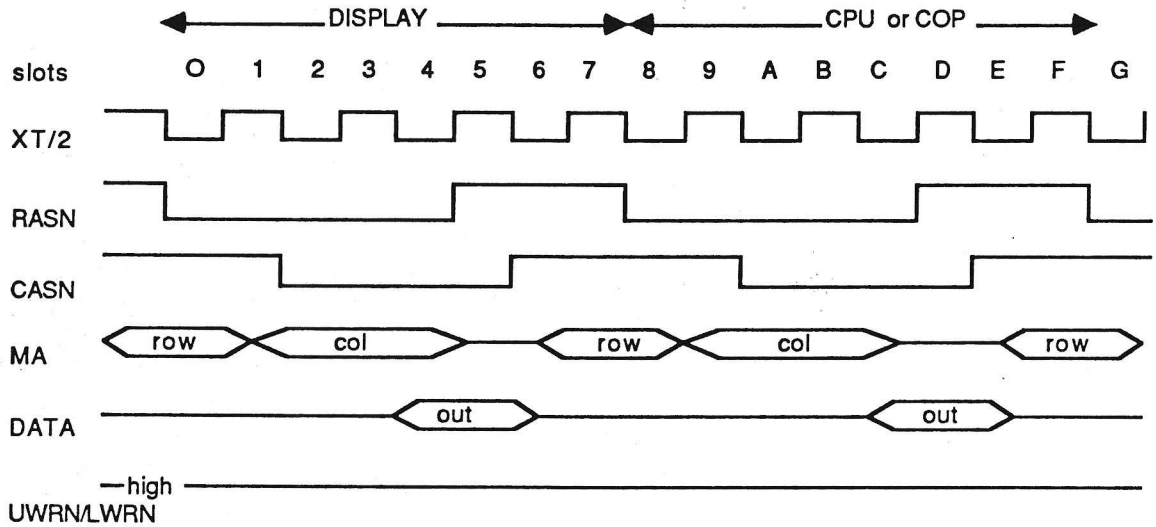
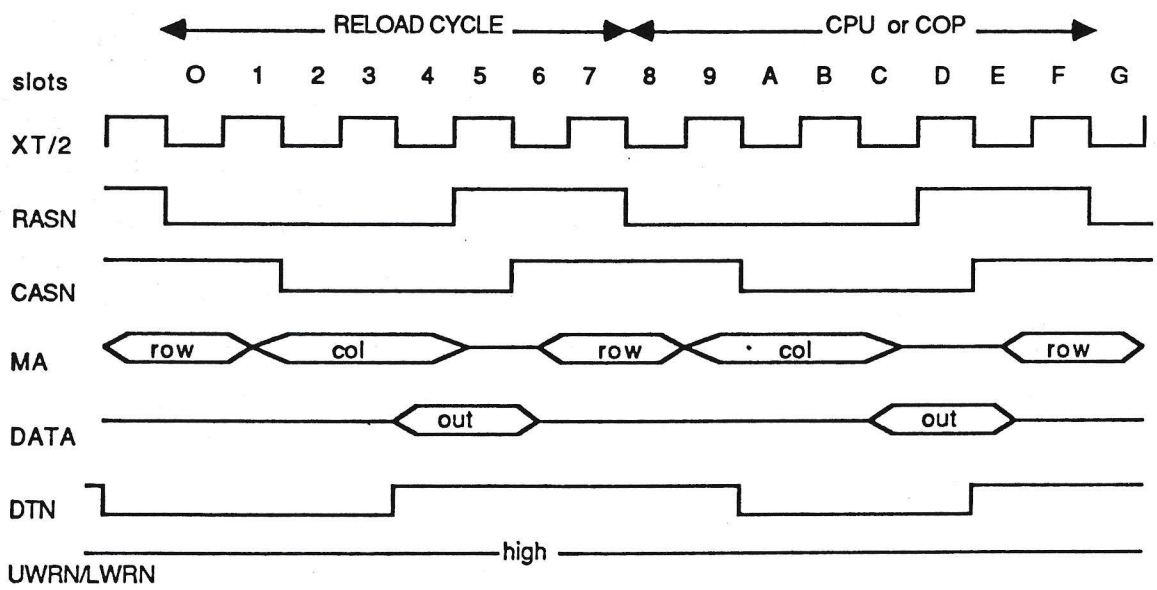


FIGURE 17 represents the beginning of a display line when using **DUAL PORT videorams**. The first access for the line is for reloading the internal shift registers. For that, the DTN signal is asserted one time slot before the falling edge of RAS and it rises one time slot before the rising edge of RASN. The rest of the time DTN=CASN and the windows, except for the refresh and the ICA/DCA part, are all given to the CPU or the coprocessor, increasing the access transparency. In this timing chart the CPU access is a read cycle.

FIGURE 17:



DRAM REFRESH

The refresh of the DRAM is made during the display time simply by connecting the LSBs of the video scan counter to the ROW addresses of the DRAM. During the vertical retrace period, the BPCRT2 will generate 4 refresh cycles during the horizontal retrace. A special Refresh counter is used for this.

In Physical screen mode, the addresses are scanned consecutively during the display active period so this principle assures that the 256 rows of the memory will be refreshed every 4 mS. When using subscreens by reloading the VSR register, one of 2 consecutive subscreens must have at least 4 lines to insure the memory refresh.

In Logical sreen mode, the addresses are generated more randomly. Four refresh cycles are then generated during each horizontal retrace.

For MOSAIC and RUN-LENGTH Mode

DRAM DESELECT.

During the RESET period, the CASxN output pins are three-stated in order to test if a memory bank is effectively connected to the device. If a zero is present (pin grounded via a resistor), the bank will be disabled and the DTACKN will not be generated. Eventually, if no DTACKN is generated by another slave or memory, the watch-dog timer will generate a BERR. All the CASxN pins are tested following this principle.

The BANK selection has an influence on the ICA pointer as indicated in this table :

TABLE 11

	256K		64K	
	BANK 1 enabled	BANK 1 disabled	MASTER	SLAVEDUAL
ICA POINTER	H400	H80400	H400	H80400

In 256K mode, the address H80400 is in the BANK 2, this means that BPCRT2 must have BANK 1 or BANK 2 enabled when using ICA.

In 64K mode, the address H80400 is in BANK 1 for the SLAVEDUAL BPCRT2 (see ADDRESS DECODING), this means that the MASTER and SLAVEDUAL BPCRT2 must have by necessity BANK 1 enabled to use ICA.

PIXEL ACCELERATOR

PIXAC GENERAL DESCRIPTION

The Pixel Accelerator logic is specific hardware available to speed up the manipulation of pixel contents in memory. It is usable under host control as a memory mapped slave interface or under control of the coprocessor via the coprocessor interface.

The main functions of the PIXel ACcelerator (PIXAC) are:

- alignment of source words onto destination words using a barrel shifter
- test-of-pixel-content-and-modify
- masking of the destination pixel
- logical operations
- bit-to-pixel and pixel-to-bit transformations

The PIXAC is intended to work for 4 bits per pixel and for 8 bits per pixel memory organisations. The manipulations are always done on a 16-bit word basis, so 4 pixels or 2 pixels are processed at a time.
Special masks are available to act selectively on one or several bits of each pixel. This feature is specially useful to transcode from plane per plane organized images to the memory organisation used by BPCRT2 or in the reverse way.

The PIXAC needs a software or a firmware layer to perform its operation. It is no more than a high speed logic unit specialized in nibble or byte manipulations.

The PIXAC logic consists of three main blocks:

- The DATA path receives Source and Destination words, operates on them depending on the selected function. It is mainly based on a 16-bit Source register (A), a 32-bit Carry register (C1 and C2) , a 16-bit multiplexer/Barrel shifter and a 16-bit Destination register (B).

- The Sequencer generates control signals for the Data path. The sequences are determined by the content of a command register.

- The Mask and Shift circuit is a complement to the pixel Data Path. It performs transparency test and generation of correct control signals to implement the selective modifications into the Destination register.

Every operation performed in between access from the host or the coprocessor interface is made using the XT/2 internal clock which guarantees that the result will be ready in less than 16 time slots (533nS for 30 MHz).

FIGURE 18 describes the organisation of the PIXel ACcelerator function.

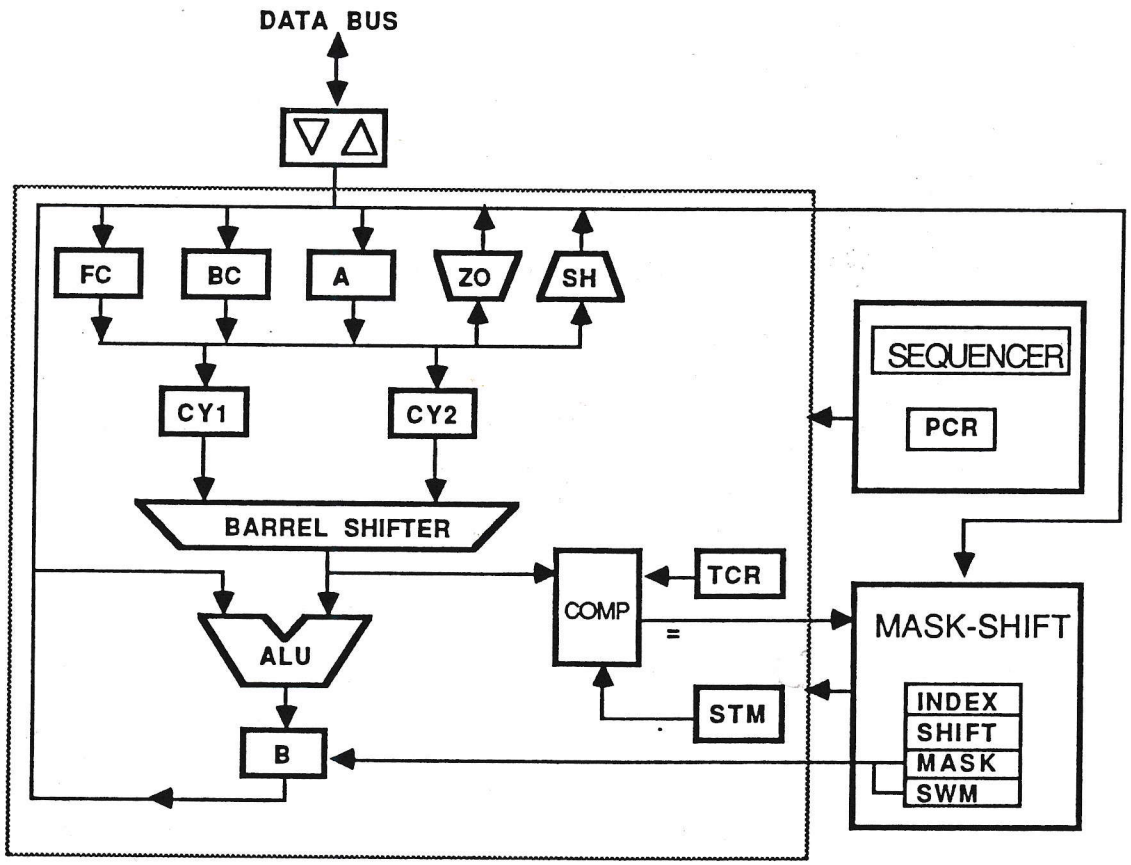


FIGURE 18: BLOCK DIAGRAM OF THE PIXEL ACCELERATOR

PIXAC OPERATIONS

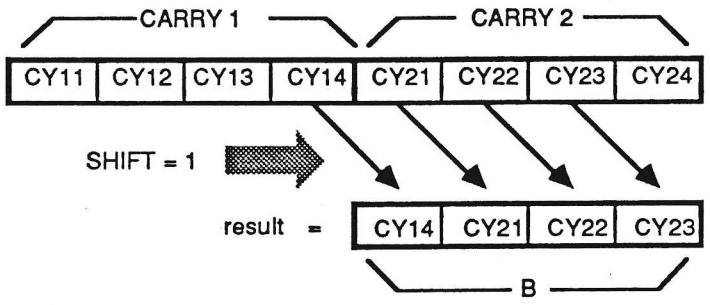
A software PIXAC driver is required to write pixels , trigger an operation and read the resulting pixels. PIXAC operations process words via the pixel path. Words are organized in 4 pixels of 4 bits or 2 pixels of 8 bits.

The pixel path has at its top the source register A, and at its bottom the destination register B. The register A must be loaded with source pixels and the B register must be loaded with destination pixels.

The PIXAC sequencer generates signals to execute operations. According to the operation type, the sequencer is triggered either by writing into A or by writing into B.

The barrel shifter of the pixel path shifts the 2 carry registers. The result is to be written into register B if there is no mask. The shift operation is always performed from left to right .

Example :



The operation result is always in the destination register B.

OPERATION DETAILS

4 main types of operations are performed :

1 . operations to copy patterns
2 . operations to exchange patterns
3 . operations to color patterns
4 . operations to compress patterns

1/ OPERATIONS TO COPY PATTERNS

COPY: Source pixels are copied into destination pixels .

PATCH: Same as COPY except that the transparent source pixels do not overwrite the respective destination pixels.

notes : > A pixel is transparent when its value is the same as the transparent color register TC.

> For clearing patterns , software can create a WRITE operation which consists of repeatedly copying a sourceword into the destination pattern .

2 / OPERATIONS TO EXCHANGE PATTERNS

EXCHANGE: Source pixels are exchanged with destination pixels.

SWAP: Same as EXCHANGE except that the transparent source pixels are not exchanged.

note : As the shift operation is only from left to right , if the nibbles in the destination word are misaligned to the left of the source word nibbles , then an apparent right-to-left shift operation must be performed by an "inverted" sequence enabled by setting a specific bit in the COMMAND register.

Example 1 :

1st source word =	|	X	|	s1	|	s2	|	s3	|
1st destination word =	|	X	|	X	|	X	|	D1	|

this sequence is normal

Example 2 :

1st source word =	|	X	|	X	|	S1	|	S2	|
1st destination word =	|	X	|	D1	|	D2	|	D3	|

this sequence must be inverted

Example 3 :

1st source word =	|	X	|	X	|	S1	|	S2	|
1st destination word =	|	X	|	X	|	D1	|	D2	|

this sequence is normal

3 / OPERATIONS TO COLOR PATTERNS

notes: Patterns can be colored by 2 different colors:
--> the foreground color which is in register FC.
--> the background color which is in register BC.

COLOR1: For non-transparent source pixels , the destination pixels are changed to the current foreground color. For transparent source pixels, destination pixels are not overwritten.

COLOR2: Same as COLOR1 except that for transparent source pixels, the destination pixels are changed to the current background color.

BCOLOR1: The source word contains bits and they are extended into pixels via the pixel path. For source bits = 1 , the destination pixels are changed to the current foreground color. For source bits = 0, the destination pixels are not overwritten. An index is used to point to the source nibble to be processed , it is automatically incremented .

Example :

		index V		
source =	nibble1	nibble2 = 1011	nibble3	nibble4
destination =	W	X	Y	Z
result in 4 bits/pixel mode =	FC	X	FC	FC
result in 8 bits/pixel mode				
after the 1st triggering =	FC		Y	Z
after the 2nd triggering =	FC		FC	

BCOLOR2: Same as BCOLOR1 except that for source bits = 0, the destination pixels are changed to the current background color.

4 / OPERATIONS TO COMPRESS PATTERNS

COMPARE: The source pixels are tested with the transparent color. The result is in the leftmost nibble of the B register.

COMPACT: Same as COMPARE except that for each test ,the result is placed in the nibble indicated by an index. The index is automatically incremented.

Example in 4 bits/pixel :

1st triggering :

source =	W	TC	TC	Z
	index V			
result =	0110	0000	0000	0000

2nd triggering :

source =	TC	X	TC	Y
		index V		
result =	0110	1010	0000	0000

Note : the previous nibble has been masked automatically and the index has been incremented.

Example in 8 bits/pixel mode:

1st triggering :

source =	TC		W	
		index V		
result =	XXXX	1010	0000	0000

2nd triggering :

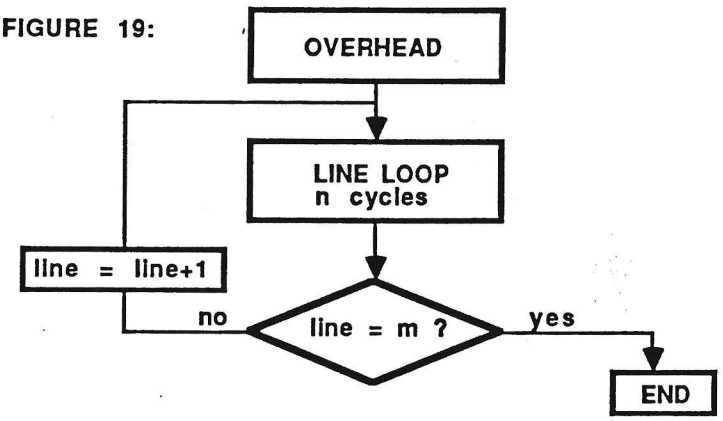
source =	Z		TC	
		index V		
result =	XXXX	1001	0000	0000

note: in 8 bits/pixel mode the 2 bits resulting from the first trigger are duplicated and a second trigger is required for a complete resulting nibble. This is also true for COMPARE .

PIXAC SOFTWARE DRIVER LOOPS

The PIXAC logic must be used with a software routine in order to perform manipulations on patterns of pixels. Considering a rectangular pattern of m lines of n words, the general flowchart is as following:

FIGURE 19:



The overhead consists of:

- Calculation of the shift to be done for alignment of source pixels of destination pixels.
- Calculation of masks to be placed at the beginning and at the end of the lines in order to protect destination pixels which are not involved in the manipulation.
- Initialization of the operation, mask, shift and color registers in PIXAC.

The loop itself consists of:

- Loading source and destination registers of PIXAC with source and destination memory contents. This action will trigger automatically the PIXAC sequencer.
- Moving back to memory the results of the manipulation.
- Counting the number of words to manipulate in the line.

When the line is finished, the software must calculate the addresses to be used for the next line to be manipulated.

The following pages will give an idea of the movements to be performed inside the inner loop.

> The loops which are described below take care only of the pixel transfers via source and destination registers. The pixel count and mask change are not considered.

> The loop entry point is not necessarily at the top.

> The loop exit point is not necessarily at the bottom.

> The syntax used to describe the movements is:

S = source word (memory location), D = destination word (memory location), A=A register, B=B register

for example: Writing into registers : D --> A or D --> B or S --> A

Reading registers : B --> D or B --> S

> According to the operation type, the pixac sequencer is triggered by writing into A or writing into B. Triggering occurence is indicated as follows:

D --> A Trigger

COPY and PATCH type B

a. basic operation

```
S -->A
D -->B          Trigger
    B --> D
```

b. operation with zoom factor 2

```
S -->A
D -->B          Trigger
    B --> D
D -->B          Trigger
    B --> D
```

COPY and PATCH type A

a.basic operation

```
D -->B
S -->A          Trigger
    B --> D
```

b. operation with shrink factor 2

```
D -->B
S -->A          Trigger
S -->A          Trigger
    B --> D
```

EXCHANGE and SWAP

a. operation with normal sequence

```
S -->A          Trigger
    B --> D
D -->A          Trigger
    B --> S
```

b. operation with inverted sequence

```
D -->A          Trigger
    B --> S
S -->A          Trigger
    B --> D
```

Note: prior to the first loop (in the overhead) it needs: D --> B

COLOR1 and COLOR2

```
S -->A
D -->B          Trigger
    B --> D
```

BCOLOR1 and BCOLOR2

note: The source nibbles are processed from left to right. At each triggering, the processed nibbles are specified.

source word = | nibble 1 | nibble 2 | nibble 3 | nibble 4 |

a. operation with shrink factor 2 in 4 bits/pixel

```
S -->A
D -->B          Trigger     nibble 1 and 2
    B --> D
D -->B          Trigger     nibble 3 and 4
    B --> D
```

b. basic operation in 4bits/pixel or operation with shrink factor 2 in 8bits/pixel

```
S -->A
D -->B          Trigger     nibble 1
    B --> D
D -->B          Trigger     nibble 2
    B --> D
D -->B          Trigger     nibble 3
    B --> D
D -->B          Trigger     nibble 4
    B --> D
```

c. operation with zoom factor 2 in 4 bits/pixel or basic operation in 8 bits/pixel

```
S -->A
D -->B          Trigger     2 MSB of nibble 1
     B --> D
D -->B          Trigger     2 LSB of nibble 1
     B --> D
   :
   :
D -->B          Trigger     2 LSB of nibble 4
     B --> D
```

d. operation with zoom factor 2 in 8 bits/pixel

```
S -->A
D -->B          Trigger     MSB of nibble 1
     B --> D
D -->B          Trigger     second MSB of nibble 1
     B --> D
D -->B          Trigger     third MSB of nibble 1
     B --> D
D -->B          Trigger     LSB of nibble 1
     B --> D
   :
   :
D --> B         Trigger     LSB of nibble 4
     B --> D
```

COMPARE

note : The feature of COMPARE is to read the result of the transparency test . In this case the concept of destination is not necessary .

```
S -->A          Trigger
   B = result
```

COMPACT

a. operation in 4 bits/pixel

```
D -->B
S -->A          Trigger
S -->A          Trigger
S -->A          Trigger
S -->A          Trigger
     B --> D
```

b. operation in 8 bits/pixel

```
D -->B
S -->A          Trigger
S -->A          Trigger
S -->A          Trigger
S -->A          Trigger
S -->A          Trigger
S -->A          Trigger
S -->A          Trigger
S -->A          Trigger
     B --> D
```

PIXAC IMPLICIT ADDRESSING

The IPA pin can be used to perform an implicit addressing of the pixel accelerator, when used by the CPU (the coprocessor already implicitly addresses PIXAC).

When the CPU uses PIXAC, it normally needs 2 instructions, one to read the memory and write into PIXAC and the other to read PIXAC and write into the memory. With the implicit addressing, a single instruction is enough.

Example with the 680XX code and COPY type A operation:

with the normal addressing :

```
MOVE.W   (A0),PIXAC_A      ; reading the source and writing it into A and triggering PIXAC
MOVE.W   PIXAC_B,(A1)      ; reading B and writing it into the destination.
```

becomes with the implicit addressing :

```
MOVE.W   (A2),(A3)         ; reading the source and implicitly writing it into A and
                             triggering PIXAC, then implicitly reading B and writing it into
                             the destination.
```

where A0 = source memory address.
A1 = destination memory address.
A2 = source memory address with IPA high.
A3 = destination memory address with IPA high.

The IPA pin has to be a MSB address (address bit A21 or greater) or the result of a MSB addresses decoding. This means that a ghost memory is necessary to perform the PIXAC implicit addressing.
For the implicit addressing, the PIXAC register which is concerned is :

--> B for the PIXAC read access
--> A or B register which triggers the PIXAC operation for the PIXAC write access.

COPROCESSOR INTERFACE

The BPCRT2 can be used with an external coprocessor to speed up the manipulation of the video memory contents. The coprocessor can request from the BPCRT2, an access to the memory or to the pixel accelerator. A coprocessor can implement a list of commands such as: copy a pattern, color, patch with test on transparency or exchange and swap areas. It can also perform drawing oriented functions like draw polyline. draw arc, fill an area or insert characters, etc...

The coprocessor can use the pixel accelerator of the BPCRT2 to speed up the manipulation. The coprocessor can also perform pixel drawing by direct access to the bit-map without using the pixel accelerator logic.

The coprocessor interface can also be used for any 68000 compatible processor, with suitable buffering.

The external coprocessor is connected to BPCRT2 via the Memory Data Bus, the Memory Address Bus and the control lines. Two hand-shake pins (CYREQN and CYACKN) are provided to request and acknowledge/synchronize the exchange of information.

INTERFACE DESCRIPTION

The coprocessor will first request access to the memory or to PIXAC by asserting the CYREQN pin. Coprocessor accesses to the memory are controlled by the BPCRT2 DRAM interface to guarantee correct memory timing. After arbitration between the various possible masters of the DRAM bus, the BPCRT2 will assert the CYACKN pin.

3 types of exchange are possible :

type A - Exchanges between coprocessor and memory
type B - Exchanges between coprocessor and BPCRT2 registers
type C - Exchanges between memory and PIXAC driven by the coprocessor

The exchange are composed of 6 phases :

PHASE 1: The BPCRT2 control arbitration for the next access.
PHASE 2: If the coprocessor has been chosen, the BPCRT2 asserts CYACKN during the CASxN assertion period of the previous access to signal the beginning of the cycle.
PHASE 3: The BPCRT2 releases CYACKN, signalling the coprocessor to put the Address and Control information on the MA and MD busses. BPCRT2 will copy the Row address information.
PHASE 4: When RAS goes low, the coprocessor releases CYREQN and the MA bus. BPCRT2 can then place the column information on MA bus. For the exchange type C, the MD bus is released and the exchange is finished. For type A and B, the MD bus is released if it is a READ cycle and active if it is a WRITE cycle(it contains the data to be written)
PHASE 5: BPCRT2 asserts CYACKN low for exchange type A and B.
PHASE 6: BPCRT2 negates CYACKN to end the transfer for exchange type A and B.

The difference between exchange type A and type B is that the CASxN signal is not generated for the exchange type B. The above exchanges are made in a completely inter-locked way to allow for shifts due to the speed of the devices.

The next page shows 2 timing charts, FIGURE 20 shows a write cycle for exchange type A or B, FIGURE 21 shows a read cycle for exchange type C (the memory is read and PIXAC is written).

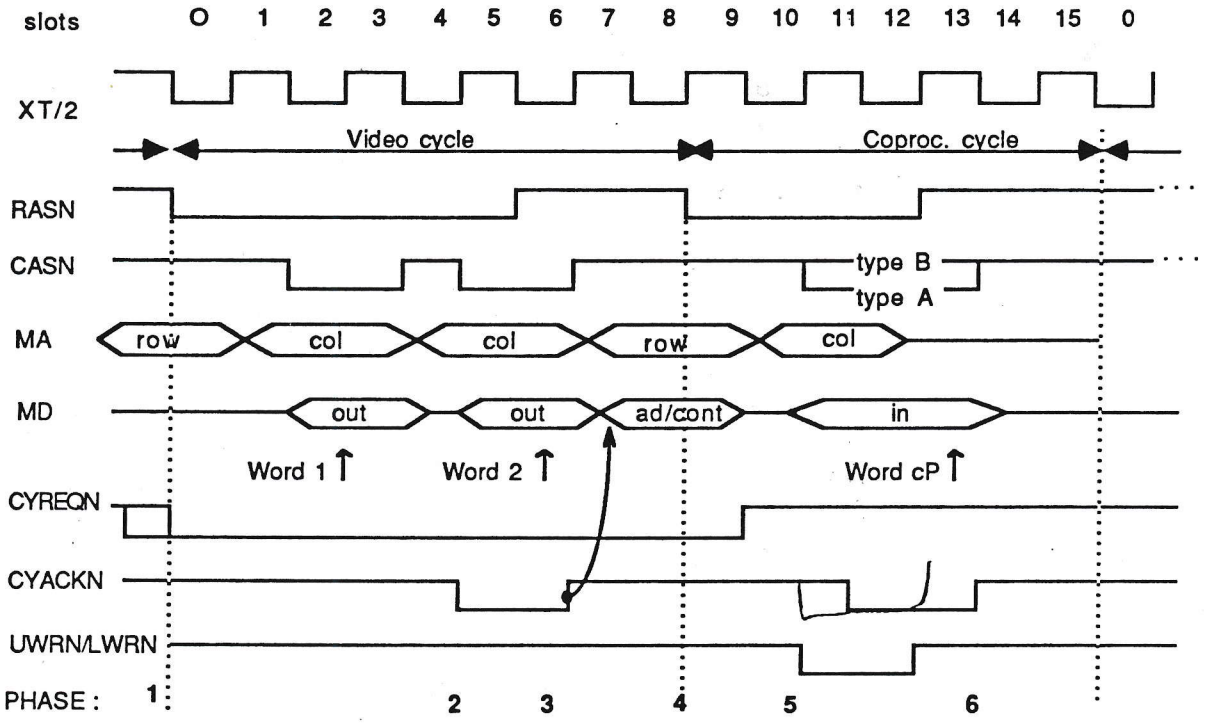


FIGURE 20: TIMING COP <---> MEMORY or BPCRT2 registers (type A or B)

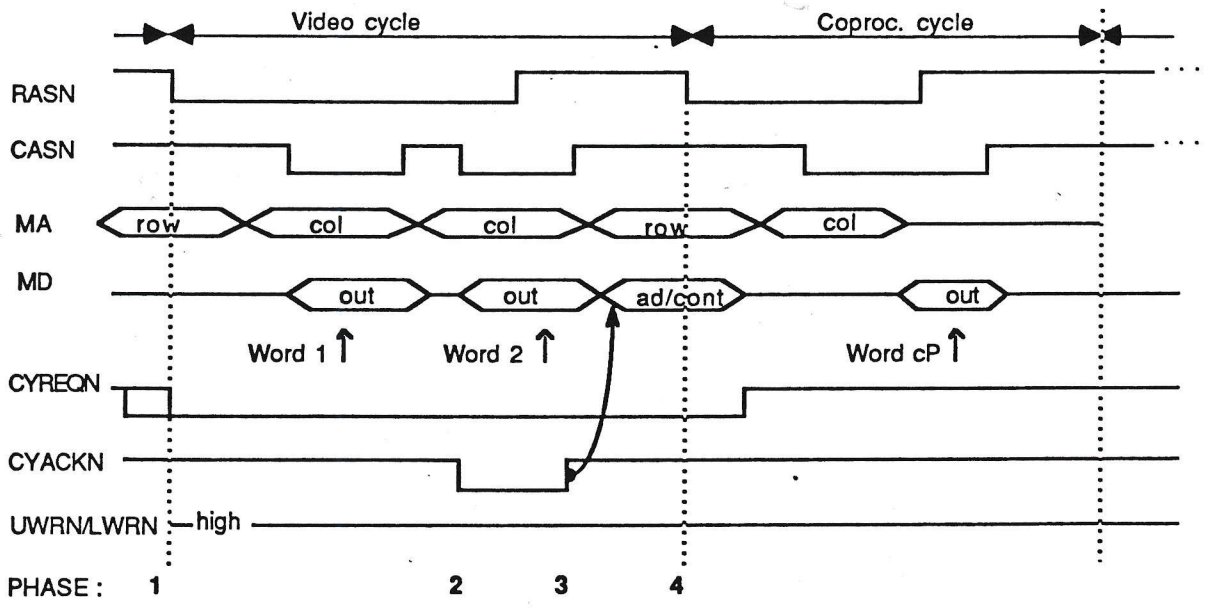


FIGURE 21: TIMING MEMORY <---> PIXAC (type C)

ad/cont = address and control word

The information to be sent by the coprocessor to the BPCRT2 consists of:

- the word address (20 bits for the 256K DRAMs, 18 bits for the 64K DRAMs).
- the Read/Write information from the coprocessor (2 bits to work at byte level).
- the direct selection of the A and B Registers of the PIXAC, SELA or SELB. If one of these signal are asserted, then the exchange type C is performed, otherwise it is an exchange type A or B.

The coprocessor must place address and control information on the Memory Address Bus MA and Memory Data Bus MD on the rising edge of CYACKN.
The Memory address bus MA contains the row address to be used immediately for the DRAM access.
The Memory Data bus MD contains the rest of the information.

Depending on the type of memory used, the correspondance between information coming from the coprocessor and MA/MD busses is indicated in this table:

TABLE 12:

	256K DRAM				64K DRAM			
COP INFO	NORMAL	NIBBLE	PAGE	VRAM	NORMAL	NIBBLE	PAGE	VRAM
A1	MA0 R	MA0 R	MD0 C	MD0 C	MA0 R	MA0 R	MD0 C	MD0 C
A2	MA1 R	MA1 R	MA1 R	MD1 C	MA1 R	MA1 R	MA1 R	MD1 C
A3	MA2 R	MA2 R	MA2 R	MD2 C	MA2 R	MA2 R	MA2 R	MD2 C
A4	MA3 R	MA3 R	MA3 R	MD3 C	MA3 R	MA3 R	MA3 R	MD3 C
A5	MA4 R	MA4 R	MA4 R	MD4 C	MA4 R	MA4 R	MA4 R	MD4 C
A6	MA5 R	MA5 R	MA5 R	MD5 C	MA5 R	MA5 R	MA5 R	MD5 C
A7	MA6 R	MA6 R	MA6 R	MD6 C	MA6 R	MA6 R	MA6 R	MD6 C
A8	MA7 R	MA7 R	MA7 R	MD7 C	MA7 R	MA7 R	MA7 R	MD7 C
A9	MA8 R	MA8 R	MA8 R	MD8 C	MA8 C	MA8 C	MA8 C	MA7 R
A10	MD0 C	MD0 C	MA0 R	MA0 R	MD0 C	MD0 C	MA0 R	MA0 R
A11	MD1 C	MD1 C	MD1 C	MA1 R	MD1 C	MD1 C	MD1 C	MA1 R
A12	MD2 C	MD2 C	MD2 C	MA2 R	MD2 C	MD2 C	MD2 C	MA2 R
A13	MD3 C	MD3 C	MD3 C	MA3 R	MD3 C	MD3 C	MD3 C	MA3 R
A14	MD4 C	MD4 C	MD4 C	MA4 R	MD4 C	MD4 C	MD4 C	MA4 R
A15	MD5 C	MD5 C	MD5 C	MA5 R	MD5 C	MD5 C	MD5 C	MA5 R
A16	MD6 C	MD6 C	MD6 C	MA6 R	MD6 C	MD6 C	MD6 C	MA6 R
A17	MD7 C	MD7 C	MD7 C	MA7 R	MD7 CAS	MD7 CAS	MD7 CAS	MA8 CAS
A18	MD8 C	MD8 C	MD8 C	MA8 R	MD8 CAS	MD8 CAS	MD8 CAS	MD8 CAS
A19	MD9 CAS	MD9 CAS	MD9 CAS	MD9 CAS	----------Not used----------			
A20	MD10 CAS	MD10 CAS	MD10 CAS	MD10 CAS	----------Not used----------			
	-------Not used----------							
SELA	MD12	MD12	MD12	MD12	MD12	MD12	MD12	MD12
SELB	MD13	MD13	MD13	MD13	MD13	MD13	MD13	MD13
R/W l b	MD14	MD14	MD14	MD14	MD14	MD14	MD14	MD14
R/W h b	MD15	MD15	MD15	MD15	MD15	MD15	MD15	MD15

A1 to A20 are the coprocessor address bits (word address).
R/W h and l are the write signal (active low) for respectively the higher and the lower byte of the DRAM bus.
SELA and SELB are asserted for the EXCHANGE type C and correspond to a direct addressing of the PIXAC.

For each type of DRAM, the LSBs of An are routed to an MAn line to be used as a Row (R), a Column (C) information during the address sequence. The 2 MSBs of An are used to select the DRAM BANK (CASxN generation).

Note: > For Nibble mode, A8 and A0 must be swapped.
> For Page mode, A1 is presented as Column address.
> For VRAM, LSBs of address are presented as Column address.

CHARACTER GENERATOR ROM

For some text intensive applications, the character generator must be placed in a ROM area. The Pixel manipulation can be performed using the coprocessor for the fastest character insertions. In that case, it is preferable to place the ROM on the DRAM bus instead of the System bus to avoid transferring the character fonts into DRAM to be accessible by the Coprocessor. The Timing of the CAS3N output can be programmed to allow utilization of ROMs. The CSCGN signal will be used to control the data output of the ROM device. In that case, extra buffers are necessary to latch the Least significant bits of the address on RASN low and and to latch the MSBs on CASN low. The speed of a large ROM device being low, the BPCRT2 will postpone the data transfer to the next available window.
If the CHARACTER GENERATOR MODE bit (CG) is set the special ROM timing will be generated.
FIGURE 22 shows the timing of the CAS3N and CSCGN signals during a display period.

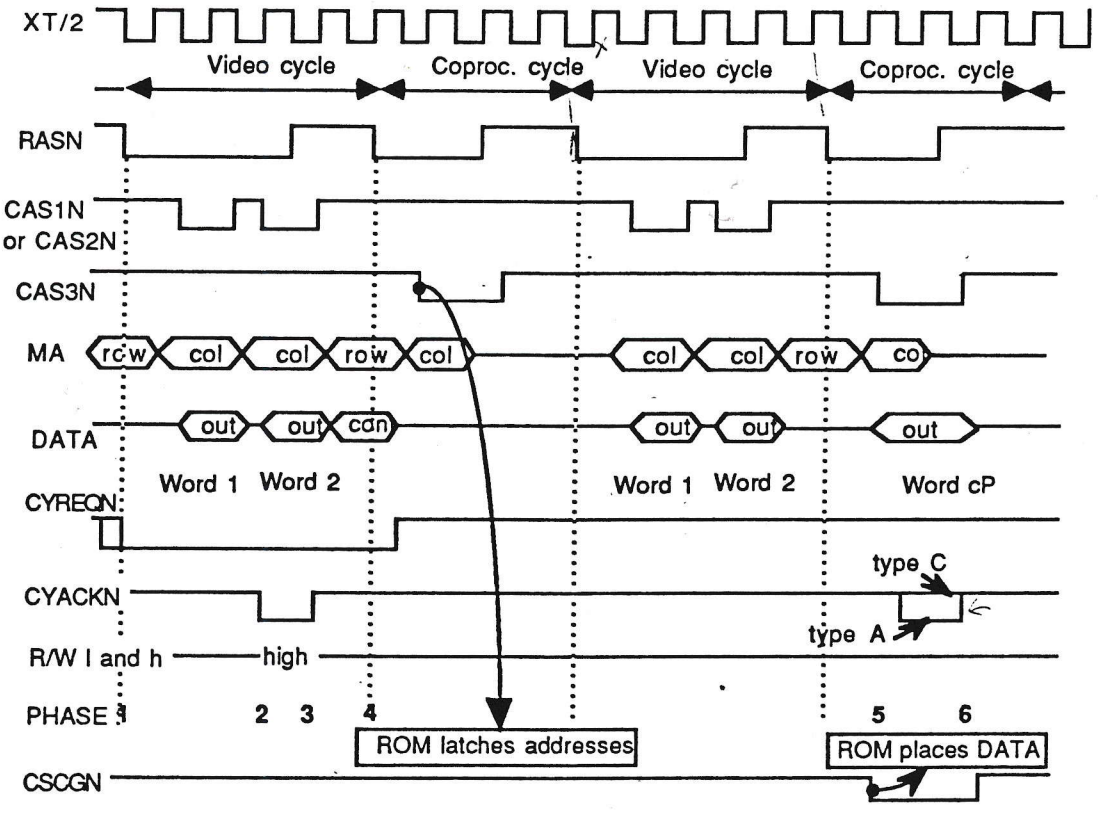


FIGURE 22: TIMING COP <---> CHAR. ROM (type A)
CHAR. ROM <---> PIXAC (type C)

BPCRT2 PROGRAMMER'S MODEL

The BPCRT2 is controlled by a set of registers accessible as memory locations. Several registers are available for the system control, the display control and the PIXAC control.

The following chapter will describe the role of each available register and the function of the bits inside these registers.

SYSTEM ORIENTED REGISTERS

CONTROL and STATUS REGISTER CSR

This register controls the system related functions of the device. It is written as a CONTROL word and read as a STATUS byte. It is reset during the initialization sequence.

CSR WRITE 1FFFE0	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EN1	EN2				EW	DD1	DD2	DM1	DM2	TD	CG	DD	ED	ST	BE

EN1-EN2 enables the INTN pin for the respective IT1 and IT2 bits (see STATUS register).

EW when set, the DTACK for a write cycle is generated 2 slots (66nS at 30 Mhz) before the DTACK for the read cycle

DD1-DD2 active when DD=1. These 2 bits permits 4 different delays for the DTACK generation when the CPU accesses the SYSTEM ROM.

DD	DD1	DD2	delay between REQUEST and DTACK generation in slots (1 slot=33nS at 30 Mhz).
1	0	0	0 --> 2
1	0	1	4 --> 6
1	1	0	8 --> 10
1	1	1	12 --> 14
0	X	X	16 --> 18

DM1-DM2 control the mode of access to the DRAM devices. The following configurations are possible:

DM1	DM2	TIMING SPEED	DRAM MODE
0	0	SLOW	NORMAL MODE
0	1	FAST	PAGE MODE
1	0	FAST	NIBBLE MODE
1	1	SLOW	DUAL PORT VIDEO RAM

TD (TYPE of DRAM) to be 0 for 64K devices and 1 for 256K devices.

CG Enables the character generator mode when set to 1. In this case the timing of the CAS3 and the CSCG pins change to be ROM compatible.

DD see DD1- DD2

ED (Early Dtack) selects how DTACK will be asserted on DRAM access from the system bus. If ED bit = 0, DTACK will be asserted when Data is available on system bus. If ED is high, an EARLY DTACK will be generated. The DTACK will be asserted two slots (66nS at 30 MHz) before data valid. For the timing chart, see DTACK GENERATION page 22.

ST (STandard EBU) when set, the width of the BLANKN period can be 720 pixels instead of 768 pixels
A pull-down resistor has to be put on the BLANKN pin.

BE (BUS ERROR ENABLE) when set, this bit activates the Watch Dog timer and the BERR generation

When the same location is read by the CPU, the following information is available:

CSR READ 1FFFE0	7	6	5	4	3	2	1	0
	DA	FG	PA			IT2	IT1	BE

DA can be polled to see if the display is active. This bit is the VERTICAL DISPLAY ACTIVE information. When low, it indicates that the display controller is not fetching information from the video memory. It does not change on each horizontal retrace. Must be used to guarantee that manipulations will have no undesirable effects on the screen.

FG This bit is set when the frame grabbing is enabled by setting FG = 1 in the DCR register, it is reset at the end of the grabbing period which can last 1 or 2 frames.

PA This bit indicates the frame PARITY when the scan mode is in interlace or interlace field repeat mode. It is 1 for the odd frame and 0 for the even frame.

IT1 This bit can be set by the DCA mechanism to generate an interrupt to the CPU. At the same time the INT pin goes low. The INTN pin is for CPUs as 68070 which have level sensitive interrupt without acknowledge. The IT1 bit and the INTN pin will be automatically reset when the CPU reads the status register. The INTN pin is not asserted if EN1 = 0.

IT2 This bit can be set by the coprocessor by zeroing the bits 14 to 11 of the Pixac Command Register (PCR). This action tells the CPU the PIXAC is free and generates an interrupt by asserting the INTN pin. The pin is reset when CPU reads the status register. The bit is reset when there is an opcode into the PCR register (one of bits 14 to 11 is set to 1). The INTN pin is not asserted if EN2 = 0.

BE is set when a BUS ERROR condition has been generated by the Watch-Dog timer. This bit is automatically reset after the read operation.

DISPLAY ORIENTED REGISTER

DISPLAY COMMAND REGISTER DCR

The Display Control Register(DCR) groups control bits for the display and 4 MSBs of the Video start address. All the bits are reset to 0 after the RESET sequence.

DCR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1FFFE2	DE	CF1	CF2	FD	SM	SS	LS	CM	FG	DF	IC	DC	VSR (MSBs) A19	A18	A17	A16

DE DISPLAY ENABLE, enables the display controller when set to 1.

CF1-CF2 must be programmed as a function of the crystal oscillator frequency as following:

CF1	CF2	FREQUENCY
0	0	19.6608 MHz
0	1	24 MHz
1	0	28.5 MHz
1	1	30 MHz

FD controls the FRAME DURATION . When reset to 0, a 50 Hz scan is generated. When set to 1, a 60 HZ scan frequency is generated.

SM, DF These 2 bits are used to select the scan mode (see page 8):

SM	DF	SCAN MODE
0	0	NON INTERLACE
0	1	DOUBLE FREQUENCY
1	0	INTERLACE
1	1	INTERLACE FIELD REPEAT

SS controls the SCREEN SIZE. When set a full screen display is generated, if reset a display with borders is generated.

LS This bit is used to choose between a LOGICAL SCREEN (LS=1) or a PHYSICAL SCREEN (LS=0). A Logical screen takes 512 Bytes per video line whatever the status of CF1 and CF2 is.

CM is the COLOR MODE bit. If set the 4 bits per pixel mode is entered. If equal to zero the 8 bits per pixel mode is active.

FG controls the FRAME GRABBING activity. When set it will provoke a grabbing activity during the next frame (or the 2 next frames). It is automatically reset after the operation.

IC, DC These 2 bits enable the ICA and DCA mechanisms (see page 11).

IC	DC	
0	0	no ICA, no DCA
0	1	ICA, REDUCED DCA MODE (DCA size = 16 bytes)
1	0	ICA, no DCA
1	1	ICA, DCA (DCA size = 64 bytes)

A19-A16 Most Significant Bits of the Video Start Address, acting in conjunction with the VSR.

DISPLAY COMMAND REGISTER 2 DCR2

This second DCR contains control bits for the display and files to be displayed, and the 4 MSB bits of the DCA pointer. All the bits are reset to 0 after the RESET sequence.

DCR2	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1FFFE8				ID	MF1	MF2	FT1	FT2					A19	A18	A17	A16

0

ID Independant DCA bit. When reset to O, enables the Interleaved DCA. When set to 1, enables the Independant DCA.

MF1-MF2 MOSAIC FACTOR bits which set the horizontal MOSAIC factor.

MF1	MF2	MOSAIC FACTOR
0	0	2
0	1	4
1	0	8
1	1	16

FT1-FT2 File Type bits which set the type of file to be displayed.

FT1	FT2	FILE TYPE
0	X	NORMAL (BIT MAP)
1	0	RUN-LENGTH
1	1	MOSAIC

A19-A16 Most significant bits of the DCA pointer. (DCP)

VIDEO START REGISTER VSR

This 16 bit register plus the bits in DCR[3:0] gives a 20 bit VIDEO START REGISTER which points to the begining of the DRAM, thus the start of the display can be located anywhere in the first Megabyte of DRAM (BANKS 1 and 2). The address is always Long Word aligned but a 2 bit offset can be specified for rolling purposes. Scrolling, Rolling and subscreens can be implemented by modification of this value on-the-fly. The contents of the register are loaded into the video counter at the begining of each frame and can be reloaded any time after this to point to the start of the next line. The VSR can also be used to jump to another ICA during the vertical retrace.

VSR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1FFFE4	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0

DCA POINTER DCP

This 14 bit register plus the bits in DCR2[3:0] gives a 18 bit DCA pointer. The DCA pointer is longword aligned, the 2 LSBs are therefore not necessary. The DCA addressing range is 1 Megabyte (BANKS 1 and 2).

DCP	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1FFFEA	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2		

BORDER COLOR REGISTER BCR

This 8 bit register contains the BORDER color. In 4 bits per pixel mode, only bits[7:4] are significant.

BCR	7	6	5	4	3	2	1	0
1FFFE7	B7	B6	B5	B4	B3	B2	B1	B0

PIXAC REGISTERS

This table indicates all the PIXel ACcelerator registers with their respective address and organization.

TABLE 13:

ACRONYM	REGISTER	ADDRESS	BITS	ORGANIZATION	R/W
				FEDCBA9876543210	
A	source register	1FFFF0	16	XXXXXXXXXXXXXXXX	W
B	destination register	1FFFF2	16	XXXXXXXXXXXXXXXX	R/W
COMMAND (PCR)	command or opcode register	1FFFF4	15	XXXXXXXXXXXXXXX-	W
MASK	mask register	1FFFF7	4	----------XXXX	W
SHIFT	shift register	1FFFF8	2	------XX--------	W
INDEX	index register	1FFFFB	2	----------XX	W
FC	foreground color register	1FFFFC	8	XXXXXXXX--------	W
BC	background color register	1FFFFD	8	--------XXXXXXXX	W
TC	transparent color register	1FFFFE	8	XXXXXXXX--------	W
SWM	selective write mask register	1FFFEC	8	XXXXXXXX--------	W
STM	selective test mask register	1FFFEF	8	--------XXXXXXXX	W

NOTE : FC, BC, TC, SWM and STM are 8 bit registers whose 4 MSBs and 4 LSBs must be identical in 4 bits/pixel mode.

A REGISTER

Register A is a 16-bit DATA register which must be loaded with the source word to be processed . For the EXCHANGE function , it must contain alternately the source and destination word. Certain functions are triggered by writing into A.

B REGISTER

Register B is a 16-bit DATA register which must be loaded with the destination word before the pixels are processed . At the end of the process, the result is available in this register . Certain functions are triggered by writing into B.

PIXAC COMMAND REGISTER

This 15 bit register is loaded prior to any manipulation. It indicates the required operation. The following table describe the bits of this register:

TABLE 14:

bit	name	Function
15	4N	0 --> 4 bits by pixel mode 1 --> 8 bits per pixel mode
14	COL	1 --> enables the COLOR and BCOLOR functions.
13	EXC	1 --> enables the EXCHANGE and SWAP functions.
12	CPY	1 --> enables the COPY and PATCH functions.
11	CMP	1 --> enables the COMPARE and COMPACT functions.
10	RTL	Set the manipulation direction in order to avoid problems when the source and destination are overlapping. Depending on the state of RTL, the effective carry register is either carry1(CY1) or carry2 (CY2). 0 --> manipulation from left to right 1 --> from right to left
9	SHK	1 --> the source size is shrunk by a factor 2. For COPY and PATCH, one source pixel out of 2 is used for the manipulation. For BCOLOR, one source bit out of 2 is used. Not used for the other functions.
8	ZOM	1 --> the source size is zoomed by a factor 2. For COPY and PATCH, each source pixel is duplicated. For BCOLOR each source bit is duplicated. Not used for the other functions.
7->4	LGF	Contains the code for 16 logical functions performed between B and the expected result from the pixel path.(see Logical Functions).
3	INV	1 --> inverts the transparency state of source pixels or source bits. Used for functions needing the transparency test. For BCOLOR1 and COLOR1, the destination pixels which are overwritten change to the current background color instead of foreground color.
2	BIT	with COP: 0 -> enables COPY type B 1 --> enables COPY type A with COL: 0 -> enables COLOR 1 --> enables BCOLOR with EXC: 0 --> normal sequence, register A is first loaded with the source word and then with the destination word. 1 --> inverted sequence, register A is first loaded with the destination word and then with the source word. with CMP: 0 --> enables COMPARE 1 --> enables COMPACT
1	TT	1 --> transparency test which allows the source pixels to be compared to the transparent color TC. If the test is positive, then the respective destination pixels are not overwritten. Used for enabling PATCH, SWAP, COLOR1 and BCOLOR1 functions.
0	NI	Used for COPY with SHRINK. This bit selects 2 out of 4 source nibbles used in the manipulation as indicated in this table: NI=0 4N=0 NI=0 4N=1 NI=1 4N=0 NI=1 4N=1 source nibbles: 0 and 2 0 and 1 1 and 3 2 and 3

PCR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1FFFF4	4N	COL	EXC	CPY	CMP	RTL	SHK	ZOM	LGF 3	LGF 2	LGF 1	LGF 0	INV	BIT	TT	NI

The pixac command register offers many possible combinations . The following table summarises all of the possibilities :

TABLE 15:

COMMAND REGISTER BITS

OPERATION	TRIG	15 4N	14 COL	13 EXC	12 CPY	11 CMP	10 RTL	9 SHK	8 ZOM	7-4 LGF	3 INV	2 BIT	1 TT	0 NI
COPY type A	A	X	0	0	1	0	X	X	0	X	D	1	0	X
COPY type B	B	X	0	0	1	0	X	O	X	X	D	0	0	0
PATCH type A	A	X	0	0	1	0	X	X	0	X	X	1	1	X
PATCH type B	B	X	0	0	1	0	X	O	X	X	X	0	1	0
EXCHANGE	A	X	0	1	0	0	0	0	0	X	D	X	0	0
SWAP	A	X	0	1	0	0	0	0	0	X	X	X	1	0
COLOR1	B	X	1	0	0	0	X	0	0	X	X	0	1	0
COLOR2	B	X	1	0	0	0	X	0	0	X	D	0	0	0
BCOLOR1	B	X	1	0	0	0	0	X	X	X	X	1	1	0
BCOLOR2	B	X	1	0	0	0	0	X	X	X	D	1	0	0
COMPARE	A	X	0	0	0	1	0	0	0	X	X	0	0	0
COMPACT	A	X	0	0	0	1	0	0	0	X	X	1	0	0

LEGEND :

TRIG: operations can be triggered by writing into A or writing into B , the name of the particular register is indicated .

X = 0 or 1 D = don't care

LOGICAL FUNCTIONS:

On top of every possible manipulation, PIXAC can perform a logical operation between the result of the pixel data path (named R) and the content of register B (named D) before loading register B with the result (named D'). The Logical Function bits (7 to 4) are used to control the logical function as following:

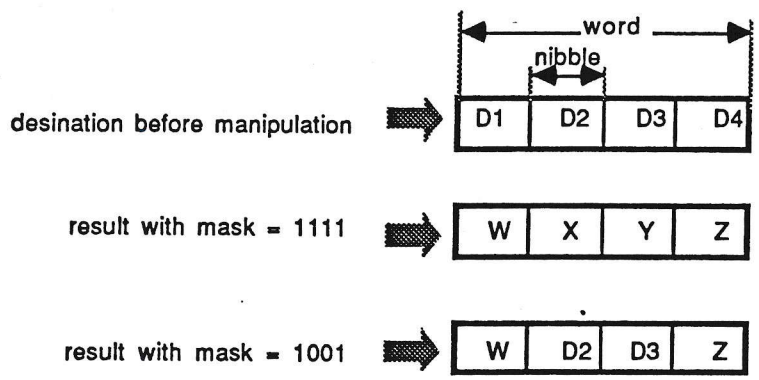
TABLE 16:

LGF 3 2 1 0	Function
0 0 0 0	D' = R
0 0 0 1	D' = NOT R
0 0 1 0	D' = 0
0 0 1 1	D' = 1
0 1 0 0	D' = NOT (D XOR R)
0 1 0 1	D' = D XOR R
0 1 1 0	D' = D AND R
0 1 1 1	D' = NOT D AND R
1 0 0 0	D' = NOT D AND NOT R
1 0 0 1	D' = D AND NOT R
1 0 1 0	D' = NOT D OR R
1 0 1 1	D' = D OR R
1 1 0 0	D' = D OR NOT R
1 1 0 1	D' = NOT D OR NOT R
1 1 1 0	D' = D
1 1 1 1	D' = NOT D

MASK REGISTER

This 4 bit register is used during the manipulation to mask the destination nibbles .

example:



note: in 8 bits/pixel mode the mask value to be used are : 0000 0011 1100 or 1111.

SHIFT REGISTER

This 2 bit register gives the value of the shift to be performed during source alignment.

```
                    source = |   s1   |   s2   |   s3   |   s4   |
                    carry  = |   cy1  |   cy2  |   cy3  |   cy4  |

result with shift = 0    :  |   s1   |   s2   |   s3   |   s4   |
result with shift = 1    :  |   cy4  |   s1   |   s2   |   s3   |
```

note : in 8 bits/pixel mode, the shift value to be used are 0 or 2.

INDEX REGISTER

For BCOLOR, it indicates which nibble in the source word is to be used.
For COMPAC, it indicates in which nibble the result must be placed.
In all cases, it is automatically incremented.
examples :

BCOLOR :

```
                    index
                      |
                      V
source = | nibble1 | nibble2 | nibble3 | nibble4 |
                      |
                      V
result = | foreground and background colors depending on nibble2 |
```

COMPACT :

```
                    index
                      |
                      V
result = |  d1  | result of |  d3  |  d4  |
                  comparison
```

FC REGISTER

This 8 bit register contains the foreground color which is used for COLOR or BCOLOR operations. In 4 bits per pixel mode, both nibbles will be used. For normal operation, the Foreground color must be loaded into FC[15:12] and in FC[11:8]. If the two values are different, the two colors will be alternately placed on consecutive pixels.

BC REGISTER

This 8 bit register contains the background color which is used for COLOR or BCOLOR operations. In 4 bits per pixel mode, both nibbles will be used. For normal operation, the Background color must be loaded into BC[7:4] and BC[3:0]. If the two values are different, the two colors will be alternately placed on consecutive pixels.

TC REGISTER

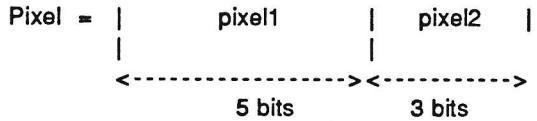
This 8 bit register contains the transparent color. In 4 bits per pixel mode, both nibbles will be used. For normal operation, the Transparent color must be loaded into TC[15:12] and TC[11:8]. If the two values are different, the two colors will be used alternately on consecutive pixels.

SWM REGISTER

This 8 bit register contains the "selective write mask". This feature enables each byte of the B register to be masked by the contents of SWM register simultaneously . This allows manipulation on groups of bits of any length up to 8 bits .

example :

In 8 bits/pixel mode, if a user wants to use 2 different screens (on different display),
For the first screen , the pixels are 5 bits wide and for the second screen, the pixels are 3 bits wide .



For manipulation into the first plane, SWM = 11111000 (binary)
For manipulation into the second plane, SWM = 00000111 (binary)

The SWM register is always acting on top of every possible function including the Logical operations. It will so guarantee that only the correct information is modified.

STM REGISTER

This 8 bit register is used as "selective test mask" register for COLOR functions. For the other functions it has an internal use , and the BC register becomes the effective STM register. The "selective test mask" feature permits the disabling of the transparency test on bits indicated by the STM register. This allows many transparent colors for the same operation , and manipulation on groups of bits of any length up to 8 bits .

example :

transparent color = 0100 1001

STM register = 1111 1100

effective transparent colors = 0100 10XX

i.e: 0100 1000
0100 1001
0100 1010
0100 1011

BPCRT2 PINNING

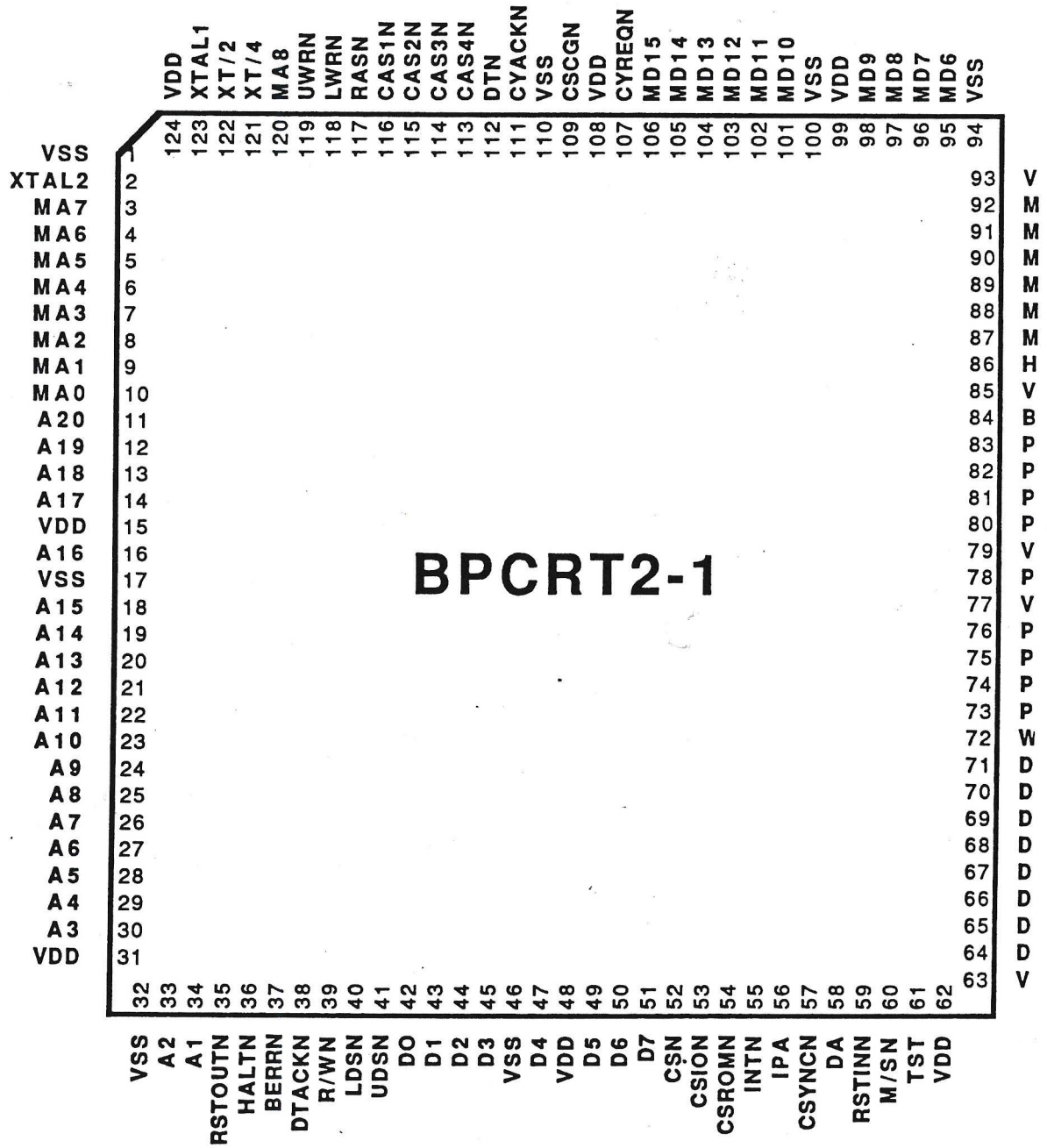


FIGURE 23: PINNING

BPCRT2 PACKAGING

The BPCRT2 is housed in a 124-pin Plastic Quad Flat Package QFP. The following drawing describes the package.

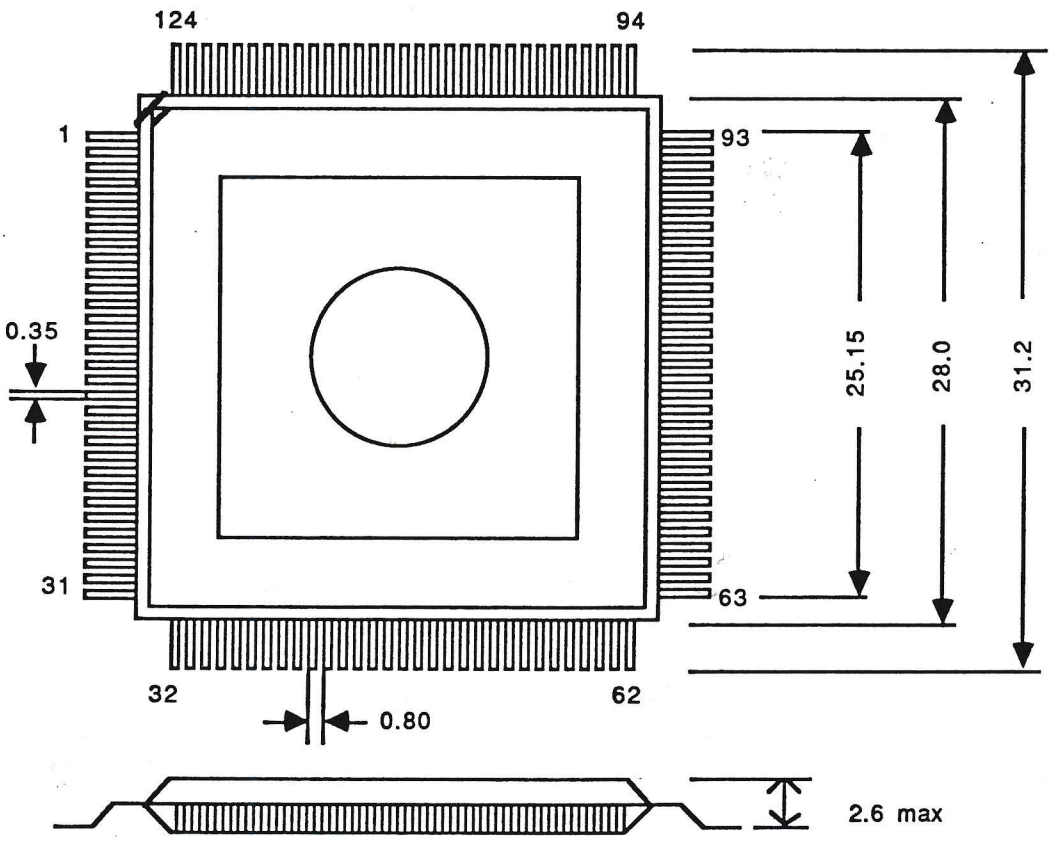


FIGURE 24: PACKAGE

ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS (Vss=0V, Ta = 25ºC)

Parameter	Symbol	min	max.	Unit
Supplyvoltage	Vdd	-0.3	+7.0	V
Input voltage	Vi	-0.3	Vdd+0.3	V
Output voltage	Vo	-0.3	Vdd+0.3	V
Output current	Io		± 20	mA
Power dissipation	Pd		500	mW
Operating temperature	Topr	0	70	ºC
Storage temperature	Tstg	-55	+150	ºC

DC CHARACTERISTICS (Vss=0, Ta=0 - 70°C)

Parameter	Symbol	Conditions	min.	typ.	max.	Unit
Supplyvoltage	V dd		4.75	5	5.25	V
Static supply current	I dds				80	µA
Operating supply current	I ddo				45	mA
Input voltage A1-20,UDS,LDS,CS,R/W, M/S,CASn,MA0-8,MD0-15 HSYNC,VSYNC,CYREQ,D0-15	V ih	Vdd=5V	2.2			V
	V il	Vdd=5V			0.8	V
Input leakage current	I li		-10		10	µA
Input current (pull-up) CASn,RSTIN	I ih	Vi=0	-1.5	-0.5	-0.15	mA
Input current XTAL1	±I if	Vi=VddorVss		3.0		µA
Output voltage D0-15,MA0-8,MD0-15,DA CSCG,DT,PCLK,WRP,CSYNC, HSYNC,VSYNC,BLANK,CYACK CSROM,CSIO,XT/2,XT/4	V oh	Io=-4mA	Vdd -0.8			V
	V ol	Io= 4mA			0.4	V
Output voltage RAS,CASn,WR1-2	V oh	Io=-8mA	Vdd -0.8			V
	V ol	Io= 8mA			0.4	V
Output leakage current	I oz	Vi=VddorVss	-10		10	µA
Input capacitance	C in	Vdd=Vi=0			10	pF
Ouptut capacitance	C out	Vdd=Vi=0			15	pF
Input output capacitance	C i/o	Vdd=Vi=0			15	pF

AC ELECTRICAL SPECIFICATION

TO BE FIXED

BPCRT2 APPLICATIONS

LAYOUT EXAMPLE

The BPCRT2 is packaged in a 124-pin package. When used with the 68070 which is a 84 pin package, the pin arrangement allows for an easy layout on a double layer printed circuit board.

The Memory interface is also optimized to reduce the length and the capacitance of the connections. A DUAL BPCRT2 application is also possible on the same principle.

FIGURE 31 shows the relative positions of the different buses involved in the connection between the two packages (46 lines).

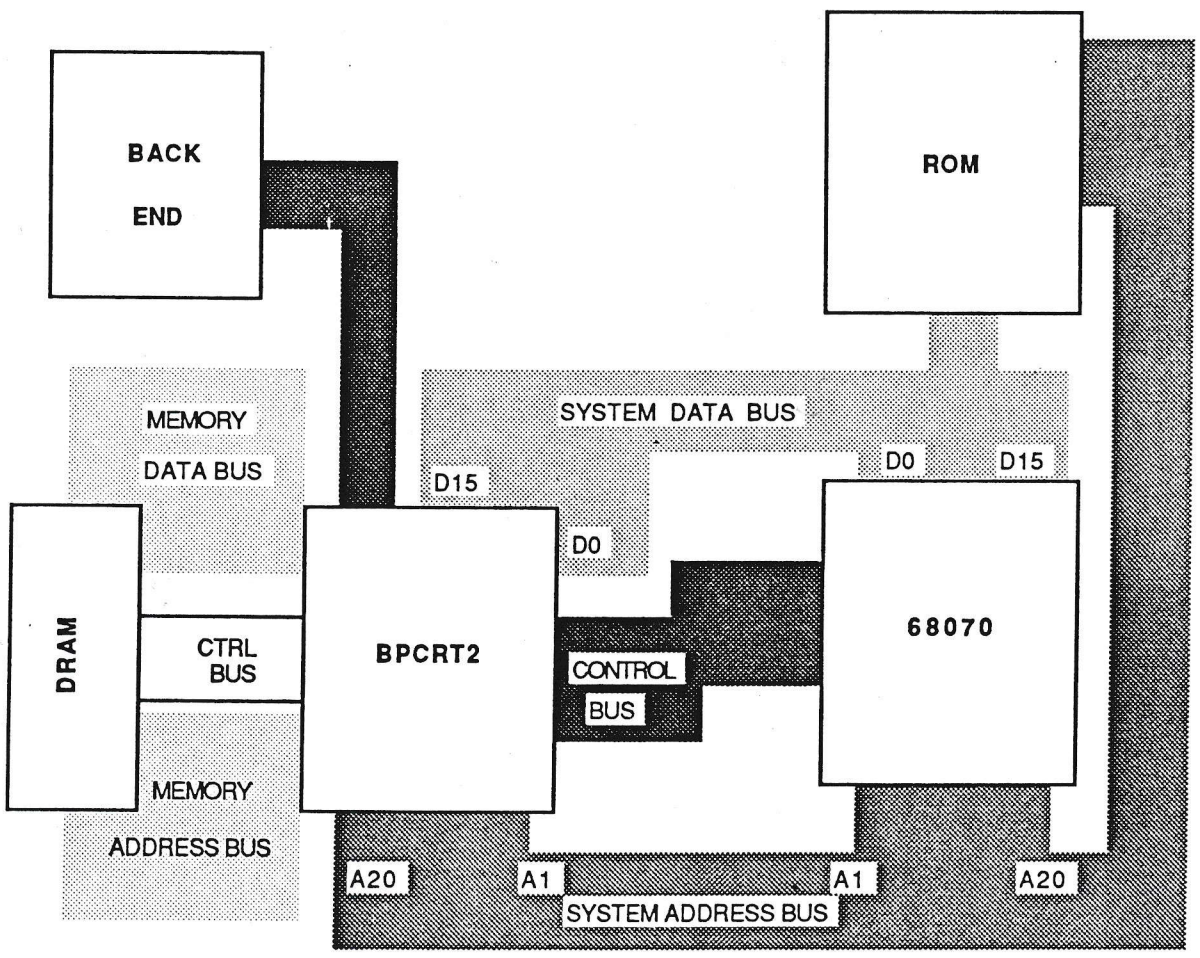


FIGURE 31: PIN ARRANGEMENT OF THE BPCRT2 USED WITH THE 68070

APPLICATION EXAMPLES

The following drawings summarise several applications envisaged for the BPCRT2 in conjunction with the 68070.

BASIC APPLICATION

This minimal computer application uses only 11 devices. It realizes an intelligent color terminal application:

CPU+MMU+DMA+I2C+UART+TIMERS ---->	68070
16-COLOR CRT+MEMORY+SYSTEM CONTROLLER --->	BPCRT2
RANDOM ACCESS MEMORY (128K Bytes) ----->	4x 64kx4 DRAM
READ ONLY MEMORY (64K Bytes) ---->	2x 32kx8 ROM
KEYBOARD/ MOUSE INTERFACE (via I2C) --->	84C00

A resolution of 512 x 280 pixels with 16 colors can be obtained. The following circuit diagram shows the main connections between ICs:

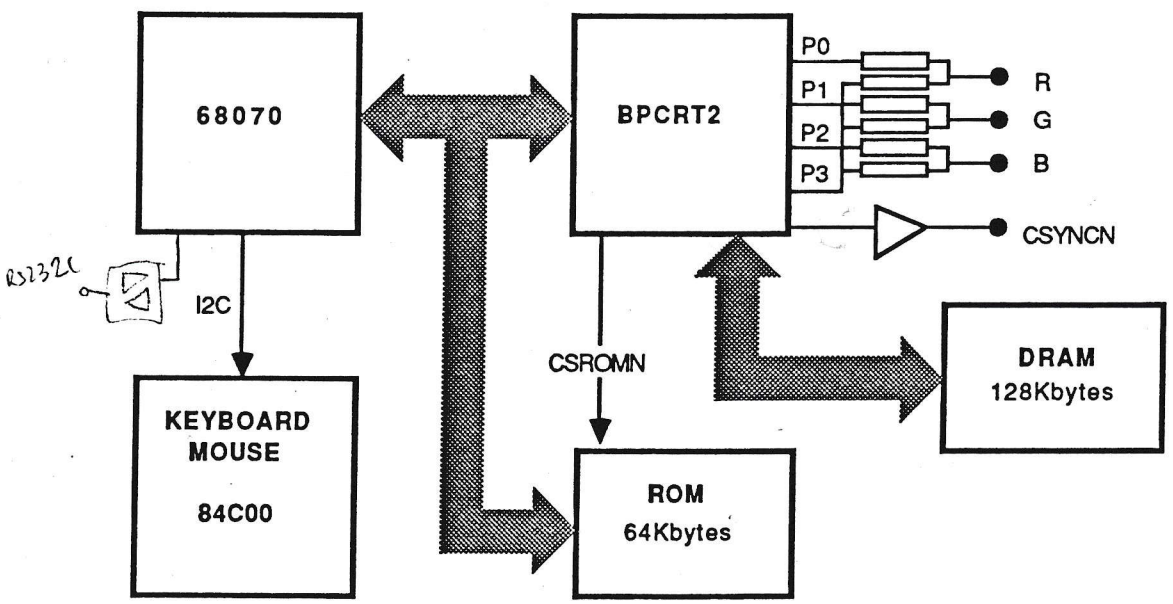


FIGURE 32: BASIC APPLICATION

EXTENDED APPLICATION

This second application is more powerful by increasing the size of the DRAM to 512 Kbytes, using 256 colors, and high speed manipulations by a coprocessor. The I/O devices are also controlled by BPCRT2.

The resolution maximum 768x560 with 4 bits per pixel or a single resolution 384x280 with 8 bits per pixel can be obtained. Using twelve 254K X 4 DRAM chips allows for 1.5 Megabyte DRAM capacity.

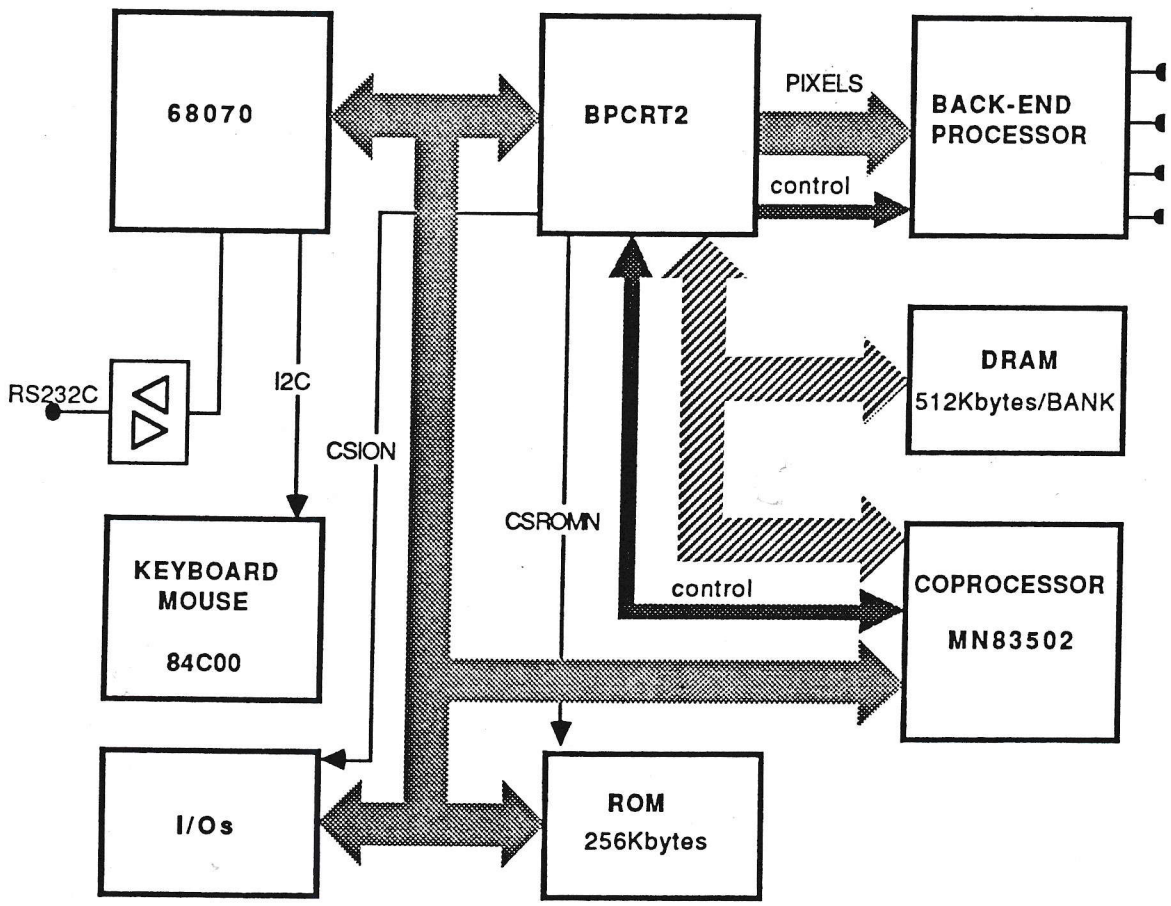


FIGURE 33: EXTENDED APPLICATION

FRAME GRABBER APPLICATION

With some extra devices a frame grabber can be implemented with real time grabbing of 384x280 pixels of 8 bits or 768x560 pixels of 4 bits performance.

The image to be grabbed can be provided by a camera, a TV or another video source.

The BPCRT2 must be in SLAVE TV mode in order to receive the external vertical synchronization. A PLL must be used to synchronize BPCRT2 with the external synchronization signals. This PLL compares the external and internal horizontal synchronization signals and generates the high frequency clock for BPCRT2.

An extra glue controls the drivers to put the grabbed information on the bus in synchronisation with the BPCRT2 scan.

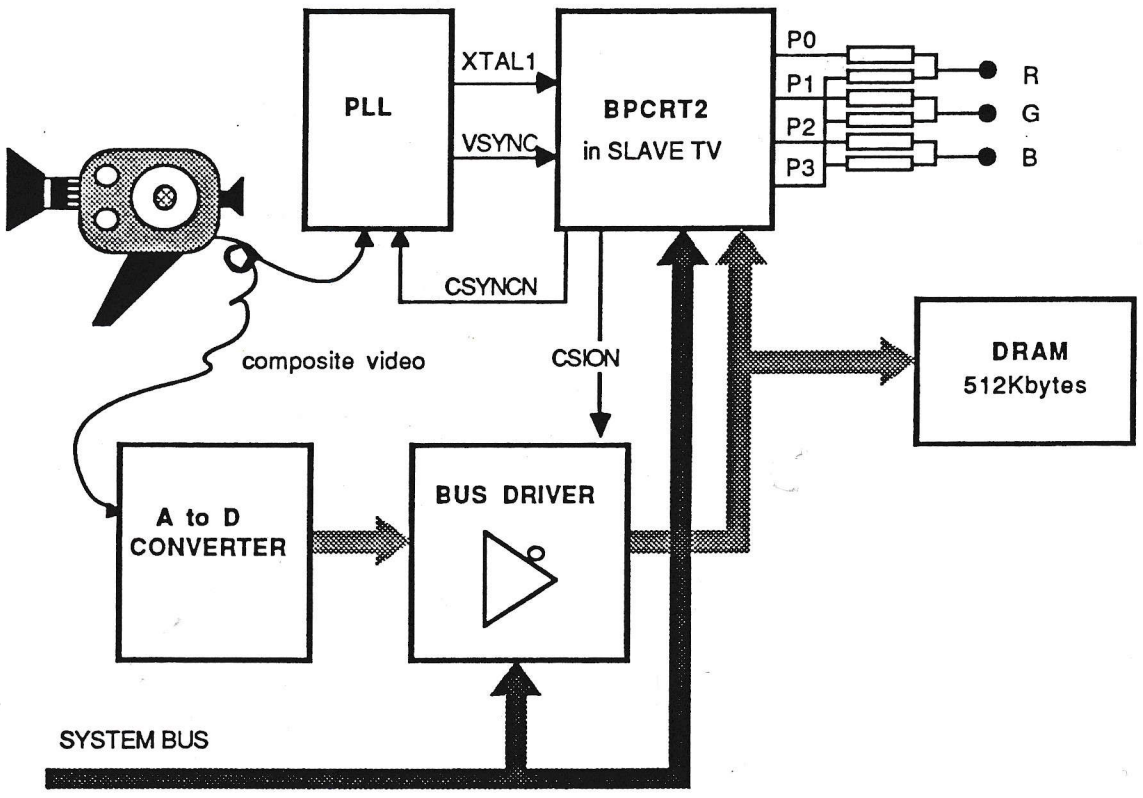


FIGURE 34: FRAME GRABBER

DUAL MODE APPLICATION

In DUAL MODE, two BPCRT2s can generate 16 bits per pixel in the 384x280 pixels mode or 8 bits per pixel in the 768x560 pixels mode. One BPCRT2 is in MASTER mode and the other in SLAVE DUAL mode, receiving the synchronization signals from the MASTER BPCRT2.

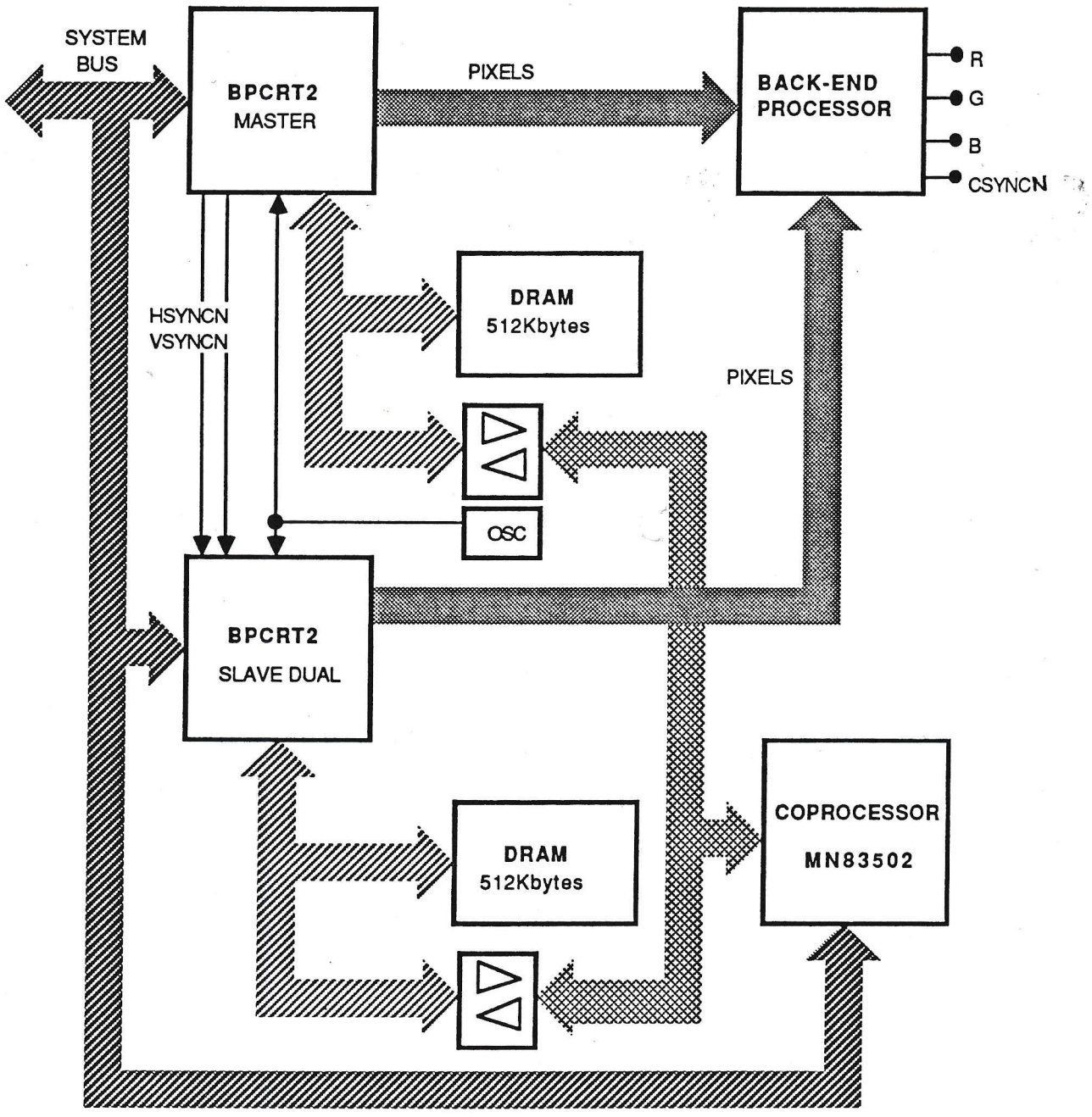


FIGURE 35: SLAVE DUAL MODE

DUAL PORT VIDEO RAM APPLICATION

When used with Dual Port Video RAM devices and in Double Frequency scan mode, the BPCRT2 can be used to implement 768 x 560 pixels with 16 different colors or 384 x 560 pixels with 256 colors. The line duration is then 32µS and the frame duration is 20 mS (16.6 mS for 480 lines).

In such a case, the additional shift registers can serialize the pixels with a 30 MHz rate.

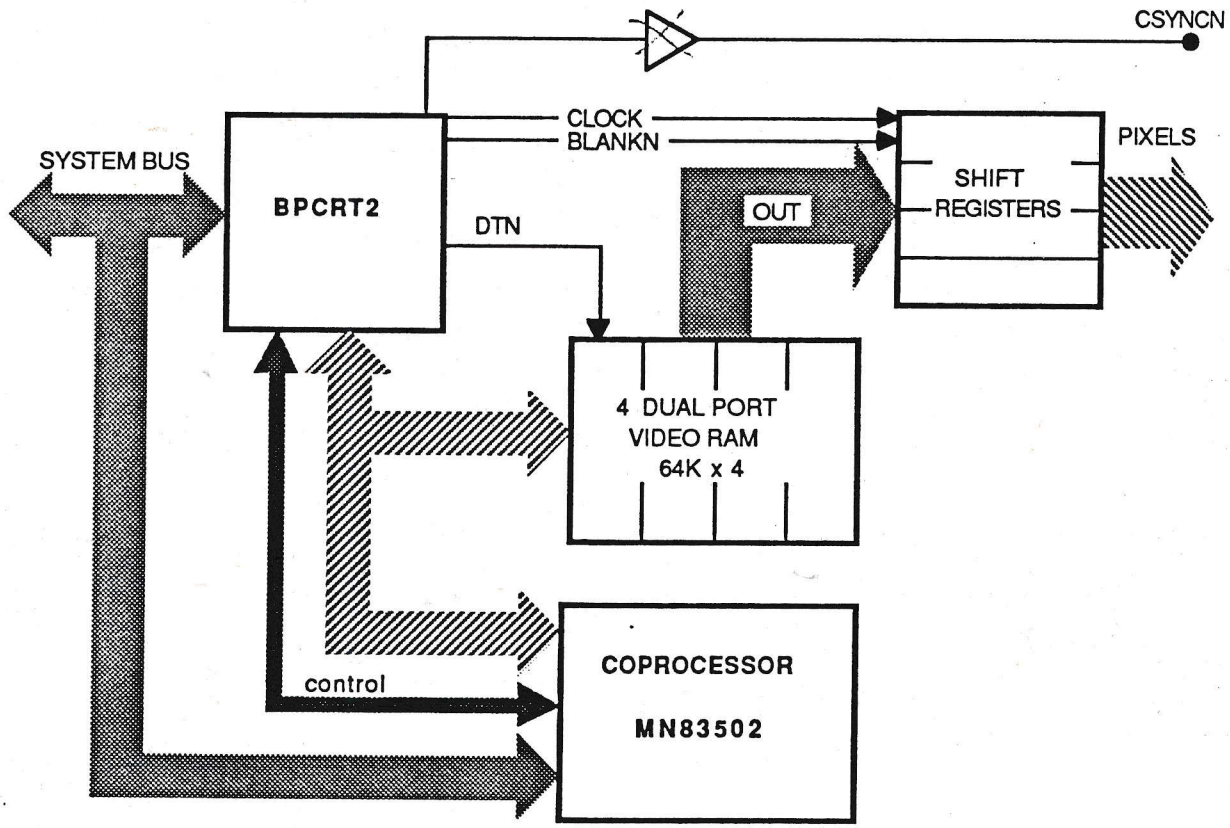


FIGURE 36: DUAL PORT VIDEORAM

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